



**PRELIMINARY**

**S6E1B8 Series**

## 32-bit ARM<sup>®</sup> Cortex<sup>®</sup>-M0+ FM0+ Microcontroller

The S6E1B8 Series is a series of highly integrated 32-bit microcontrollers designed for embedded controllers aiming at low power consumption and low cost. This series has the ARM Cortex-M0+ Processor with on-chip Flash memory and SRAM, and consists of peripheral functions such as various timers, LCD controller (LCDC), AES, ADC and communication interfaces (UART, CSIO (SPI), I<sup>2</sup>C, I<sup>2</sup>S, Smart Card, and USB). The products which are described in this data sheet are placed into TYPE2-M0+ product categories in "FM0+ Family Peripheral Manual".

### Features

#### 32-bit ARM Cortex-M0+ Core

- Processor version: r0p1
- Maximum operating frequency: 40.8 MHz
- Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 24 peripheral interrupt with 4 selectable interrupt priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

#### Bit Band Operation

Compatible with Cortex-M3 bit band operation.

#### On-Chip Memory

- Flash memory
  - Up to 512 K+48 Kbytes
  - Dual bank:
    - upper bank : 512 Kbytes(64 Kbytes x 8)
    - lower bank : 48 Kbytes(8 Kbytes x 6)
  - Read cycle: 0 wait-cycle
  - Security function for code protection
- SRAM

The on-chip SRAM of this series has one independent SRAM .

  - Up to SRAM: 60 K+4 Kbytes
  - 4Kbytes: can retain value in Deep Standby Mode

#### USB Interface

USB interface is composed of Device and Host PLL for USB is built-in, USB clock can be generated by multiplication of Main clock.

- USB Device
  - USB 2.0 Full-Speed supported
  - Max 6 EndPoint supported
    - EndPoint 0 is control transfer
    - EndPoint 1, 2 can be selected Bulk-transfer, Interrupt-transfer or Isochronous-transfer
    - EndPoint 3 to 5 can select Bulk-transfer or Interrupt-transfer
    - EndPoint 1 to 5 comprise Double Buffer
    - The size of each EndPoint is according to the follows
    - EndPoint 0, 2 to 5 : 64 bytes
    - EndPoint 1 : 256 bytes

- USB host
  - USB 2.0 Full/Low-Speed supported
  - Bulk-transfer, Interrupt-transfer and Isochronous-transfer support
  - USB Device connected/disconnected automatically detect
  - IN/OUT token handshake packet automatically
  - Max 256-byte packet-length supported
  - Wake-up function supported

#### LCD Controller (LCDC)

- Selectable from 44 SEG x 4 COM (Max) or 40 SEG x 8 COM (Max)
- Internal Charge pump can generate 4.6 V at most
- Internal divide resistor is contained (selectable from 10 kΩ or 100 kΩ for the resistor value)
- LCD drive power supply (bias) pin (VV4 to VV0)
- Interrupt function synchronized with the LCD module frame frequency
- With blinking function
- Inverted display function

#### Multi-Function Serial Interface (Max 8channels)

- 128 bytes with Tx/Rx FIFO in all channels (The number of FIFO steps varies depending on the settings of the communication mode or bit length.)
- The operation mode of each channel can be selected from one of the following.
  - UART
  - CSIO (CSIO is known to many customers as SPI)
  - I<sup>2</sup>C
- UART
  - Full duplex double buffer
  - Parity can be enabled or disabled.
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Various error detection functions (parity errors, framing errors, and overrun errors)
- CSIO (also known as SPI)
  - Full duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detection function
  - Serial chip select function (ch1 and ch3 only)
  - Data length: 5 to 16 bits

■ I<sup>2</sup>C

- Standard-mode (Max: 100 kbps) supported / Fast-mode (Max 400 kbps) supported.

■ I<sup>2</sup>S

- Using CSIO (ch.5, ch.6) and I<sup>2</sup>S clock generator
- Supports two transfer protocol
  - I<sup>2</sup>S
  - MSB-justified
- Master mode only

**Descriptor System Data Transfer Controller (DSTC) (64 Channels)**

- The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor
- system and, following the specified contents of the Descriptor that has already been constructed on the
- memory, can access directly the memory / peripheral device and performs the data transfer operation.
- It supports the software activation, the hardware activation, and the chain activation functions

**A/D Converter (Max: 24 Channels)**

- 12-bit A/D Converter
  - Successive approximation type
  - Conversion time: 2.0 μs @ 2.7 V to 3.6 V
  - Priority conversion available (2 levels of priority)
  - Scan conversion mode
  - Built-in FIFO for conversion data storage (for scan conversion: 16 steps, for priority conversion: 4 steps)

**Base Timer (Max: 8 Channels)**

The operation mode of each channel can be selected from one of the following.

- 16-bit PWM timer
- 16-bit PPG timer
- 16/32-bit reload timer
- 16/32-bit PWC timer

**General-Purpose I/O Port**

This series can use its pin as a general-purpose I/O port when it is not used for an external bus or a peripheral function. All ports can be set to fast general-purpose I/O ports or slow general-purpose I/O ports. In addition, this series has a port relocate function that can set to which I/O port a peripheral function can be allocated.

- All ports are Fast GPIO which can be accessed by 1 cycle
- Capable of controlling the pull-up of each pin
- Capable of reading pin level directly
- Port relocate function
- Up to 102 fast general-purpose I/O ports @120-pin package

- Certain ports are 5 V tolerant.

See 4. List of Pin Functions and 5. I/O Circuit Type for the corresponding pins.

**Dual Timer (32-/16-bit Down Counter)**

The Dual Timer consists of two programmable 32-/16-bit down counters. The operation mode of each timer channel can be selected from one of the following.

- Free-running mode
- Periodic mode (= Reload mode)
- One-shot mode

**Multi-Function Timer**

The Multi-function Timer consists of the following blocks.

- 16-bit free-run timer × 3 channels
- Input capture × 4 channels
- Output compare × 6 channels
- ADC start compare × 6 channel
- Waveform generator × 3 channels
- 16-bit PPG timer × 3 channels

IGBT mode is contained.

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- ADC start function
- DTIF (motor emergency stop) interrupt function

**Real-Time Clock (RTC with Vbat)**

The Real-time Clock counts year/month/day/hour/minute/second/day of the week from year 01 to year 99.

- The RTC can generate an interrupt at a specific time (year/month/day/hour/minute/second/day of the week) and can also generate an interrupt in a specific year, in a specific month, on a specific day, at a specific hour or at a specific minute.
- It has a timer interrupt function generating an interrupt upon a specific time or at specific intervals.
- It can keep counting while rewriting the time.
- It can count leap years automatically.

**Watch Counter**

The Watch Counter wakes up the microcontroller from the low power consumption mode. The clock source can be selected from the main clock, the sub clock, the built-in high-speed CR clock or the built-in low-speed CR clock.

Interval timer: up to 64 s (sub clock: 32.768 kHz)

**External Interrupt Controller Unit**

- Up to 24 external interrupt input pins
- Non-maskable interrupt (NMI) input pin: 1

**Watchdog Timer (2 Channels)**

The watchdog timer generates an interrupt or a reset when the counter reaches a time-out value.

This series consists of two different watchdogs, hardware watchdog and software watchdog.

The hardware watchdog timer is clocked by the built-in low-speed CR oscillator. Therefore, the hardware watchdog is active in any low-power consumption modes except RTC, Stop, Deep standby RTC and Deep standby Stop mode.

**CRC (Cyclic Redundancy Check) Accelerator**

The CRC accelerator calculates the CRC which has a heavy software processing load, and achieves a reduction of the integrity check processing load for reception data and storage.

- CCITT CRC16 and IEEE-802.3 CRC32 are supported.
  - CCITT CRC16 Generator Polynomial: 0x1021
  - IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

**HDMI-CEC/Remote Control Receiver (Up to 2 Channels)**

- HDMI-CEC transmitter
  - Header block automatic transmission by judging Signal free
  - Generating status interrupt by detecting Arbitration lost
  - Generating START, EOM, ACK automatically to output CEC transmission by setting 1 byte data
  - Generating transmission status interrupt when transmitting 1 block (1 byte data and EOM/ACK)
- HDMI-CEC receiver
  - Automatic ACK reply function available
  - Line error detection function available
- Remote control receiver
  - 4 bytes reception buffer
  - Repeat code detection function available

**Smart Card Interface (Max 2 Channels)**

- Compliant with ISO7816-3 specification
- Card Reader only/B class card only
- Available protocols
  - Transmitter: 8E2, 8O2, 8N2
  - Receiver: 8E1, 8O1, 8N2, 8N1, 9N1
  - Inverse mode
- TX/RX FIFO integrated (RX: 16-bytes, TX:16-bytes)

**AES Calculator**

- AES (Advanced Encryption Standard) calculator is an AES common key crypto accelerator that is compliant with FIPS (Federal Information Processing Standard Publication) 197.
- Available key length: 128/192/256-bit
- CBC mode and ECB mode support

**Clock and Reset**

- Clocks
 

A clock can be selected from five clock sources (two external oscillators, two built-in CR oscillator, and main PLL).

  - Main clock: 4 MHz to 40 MHz
  - Sub clock: 32.768 kHz
  - Built-in high-speed CR clock: 4 MHz
  - Built-in low-speed CR clock: 100 kHz
  - Main PLL clock
- Resets
  - Reset request from the INITX pin
  - Power on reset
  - Software reset
  - Watchdog timer reset
  - Low-voltage detection reset
  - Clock supervisor reset

**Clock Supervisor (CSV)**

The Clock Supervisor monitors the failure of external clocks with a clock generated by a built-in CR oscillator.

- If an external clock failure (clock stop) is detected, a reset is asserted.
- If an external frequency anomaly is detected, an interrupt or a reset is asserted.

**Low-Voltage Detector (LVD)**

This series monitors the voltage on the VCC pin with a 2-stage mechanism. When the voltage falls below a designated voltage, the Low-voltage Detector generates an interrupt or a reset.

- LVDR: monitor Vcc and auto-reset operation
- LVD1: monitor Vcc and error reporting via an interrupt
- LVD2: selectable to monitor Vcc or LVDI and error reporting via an interrupt

**Low Power Consumption Mode**

This series has six low power consumption modes.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable between keeping the value of RAM and not)
- Deep standby Stop (selectable between keeping the value of RAM and not)

### Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

### VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent VBAT pin. RTC (calendar circuit) / 32 kHz oscillation circuit. The following circuit can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

### Debug

- Serial Wire Debug Port (SW-DP)
- Micro Trace Buffer (MTB)

### Unique ID

A 41-bit unique value of the device has been set.

### Power Supply

- Wide voltage range:
  - VCC = 1.65V to 3.6 V
  - VCC = 3.0V to 3.6V (when USB is used)
  - VCC = 2.2V to 3.6V (when LCDC is used)
- Power supply for VBAT: VBAT = 1.65 V to 3.6 V

**Table of Contents**

**Features..... 1**

**1. Product Lineup..... 7**

**2. Packages..... 8**

**3. Pin Assignment..... 9**

**4. List of Pin Functions..... 12**

**5. I/O Circuit Type..... 36**

**6. Handling Precautions ..... 46**

6.1 Precautions for Product Design..... 46

6.2 Precautions for Package Mounting..... 47

6.3 Precautions for Use Environment..... 49

**7. Handling Devices ..... 50**

**8. Block Diagram ..... 53**

**9. Memory Map ..... 54**

**10. Pin Status in Each CPU State..... 57**

**11. Electrical Characteristics ..... 67**

11.1 Absolute Maximum Ratings..... 67

11.2 Recommended Operating Conditions..... 68

11.3 DC Characteristics..... 69

11.3.1 Current Rating..... 69

11.3.2 Pin Characteristics ..... 74

11.3.3 LCD Characteristic..... 75

11.4 AC Characteristics..... 79

11.4.1 Main Clock Input Characteristics..... 79

11.4.2 Sub Clock Input Characteristics ..... 80

11.4.3 Built-in CR Oscillation Characteristics..... 81

11.4.4 Operating Conditions of Main PLL (In the Case of Using the Main Clock as the Input Clock of the PLL) ..... 82

11.4.5 Operating Conditions of Main PLL (In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)..... 82

11.4.6 Reset Input Characteristics ..... 83

11.4.7 Power-on Reset Timing..... 83

11.4.8 Base Timer Input Timing ..... 84

11.4.9 CSIO/SPI/UART Timing..... 85

11.4.10 External Input Timing..... 102

11.4.11 I<sup>2</sup>C Timing..... 103

11.4.12 I<sup>2</sup>S Timing..... 104

11.4.13 Smart Card Interface Characteristics..... 105

11.4.14 SW-DP Timing..... 106

11.5 12-bit A/D Converter..... 107

11.6 USB Characteristics ..... 110

11.7 Low-Voltage Detection Characteristics..... 115

11.7.1 Low-Voltage Detection Reset..... 115

11.7.2 Low-Voltage Detection Interrupt..... 116

11.7.3 Low-Voltage Detection Interrupt 2..... 117

11.8 Flash Memory Write/Erase Characteristics ..... 118

11.9 Return Time from Low-Power Consumption Mode..... 119

11.9.1 Return Factor: Interrupt/WKUP ..... 119

11.9.2 Return Factor: Reset..... 121

**12. Ordering Information ..... 123**



13. Package Dimensions ..... 124  
Document History..... 127  
Sales, Solutions, and Legal Information..... 128

## 1. Product Lineup

### Memory Size

Product Name		S6E1B84E/F/G	S6E1B86E/F/G
On-chip Flash memory	Upper Bank	256 Kbytes	512 Kbytes
	Lower Bank	48 Kbytes	48 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes

### Function

Product Name			S6E1B84E0A S6E1B86E0A S6E1B84EHA S6E1B86EHA	S6E1B84F0A S6E1B86F0A S6E1B84FHA S6E1B86FHA	S6E1B84G0A S6E1B86G0A S6E1B84GHA S6E1B86GHA	
Pin count			80	100	120	
CPU			Cortex-M0+			
Frequency			40.8 MHz			
Power supply voltage range			1.65 V to 3.6 V			
USB 2.0 (Device/Host)			1 unit			
DSTC			64ch			
Multi-function Serial Interface (UART/CSIO (SPI)/I <sup>2</sup> C/I <sup>2</sup> S)			8ch (Max) with 128 bytes FIFO I <sup>2</sup> S: ch.5, ch.6			
Base Timer (PWC/Reload timer/PWM/PPG)			8ch (Max)			
LCD controller			20SEG x 8COM(Max) / 24SEG x 4COM(Max)	32SEG x 8COM(Max) / 36SEG x 4COM(Max)	40SEG x 8COM(Max) / 44SEG x 4COM(Max)	
Multi-function Timer	A/D activation compare	6ch	1 unit			
	Input capture	4ch				
	Free-run timer	3ch				
	Output compare	6ch				
	Waveform generator	3ch				
	PPG	3ch				
Dual Timer			1 unit			
HDMI-CEC/ Remote Control Receiver			2ch (max)			
Smart Card Interface			2ch (max)			
Real-time Clock			1 unit (with battery power)			
Watch Counter			1 unit			
CRC Accelerator			Yes			
Watchdog timer			1ch (SW) + 1ch (HW)			
External Interrupt			24 pins (Max), NMI x 1			
I/O port			65 pins (Max)	82 pins (Max)	102 pins (Max)	
12-bit A/D converter			16ch (1 unit)	23ch (1 unit)	24ch (1 unit)	
CSV (Clock Supervisor)			Yes			
LVD (Low-voltage Detection)			2ch			
Built-in CR	High-speed		4 MHz			
	Low-speed		100 kHz			
Debug Function			SW-DP			
Unique ID			Yes			
AES Calculator			-	Yes <sup>*1</sup>	-	Yes <sup>*1</sup>

\*1: AES Calculator is built in following products.

S6E1B86GHA, S6E1B84GHA, S6E1B86FHA, S6E1B84FHA, S6E1B86EHA, S6E1B84EHA

### Note:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.  
See "11 Electrical Characteristics 11.4 AC Characteristics 11.4.3 Built-in CR Oscillation Characteristics" for accuracy of built-in CR.

## 2. Packages

Product Name Package	S6E1B84E/S6E1B86E	S6E1B84F/S6E1B86F	S6E1B84G/S6E1B86G
LQFP: FPT-80P-M21 (0.50 mm pitch)	○	-	-
LQFP: FPT-100P-M20 (0.50 mm pitch)	-	○	-
LQFP: FPT-120P-M21 (0.50 mm pitch)	-	-	○

○: Available

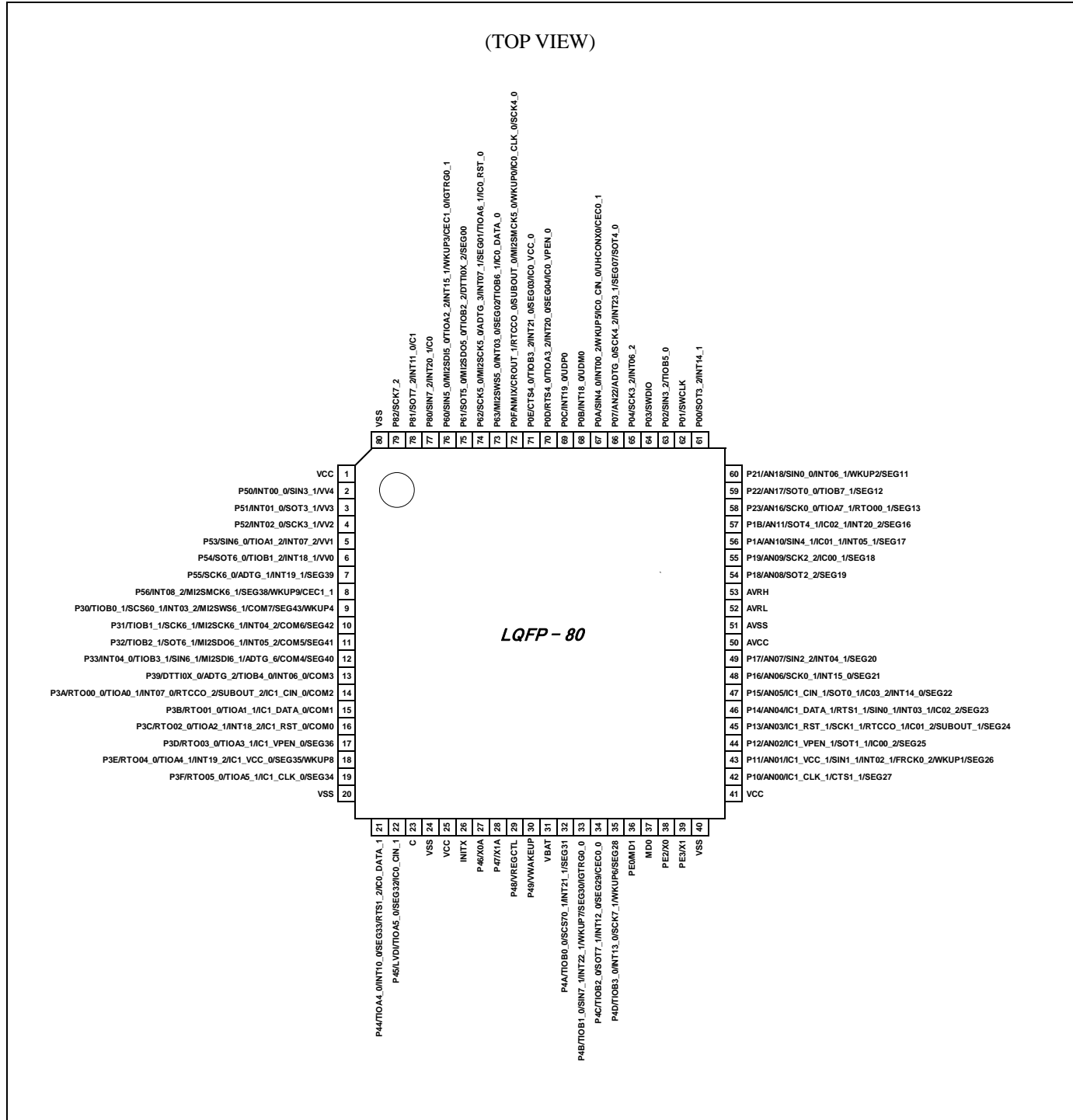
**Note:**

- See "13. Package Dimensions" for detailed information on each package.



### 3. Pin Assignment

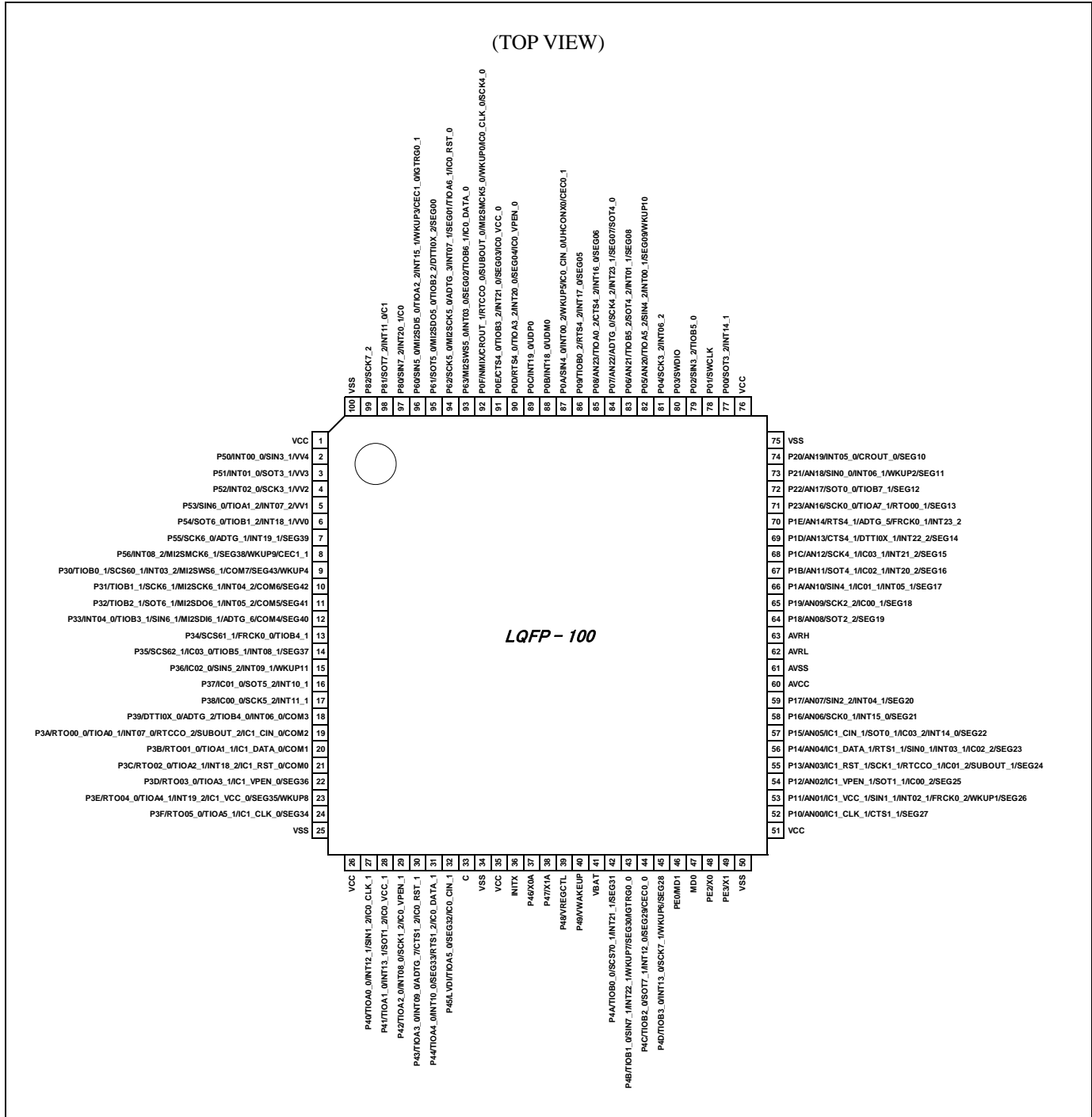
#### FPT-80P-M21



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

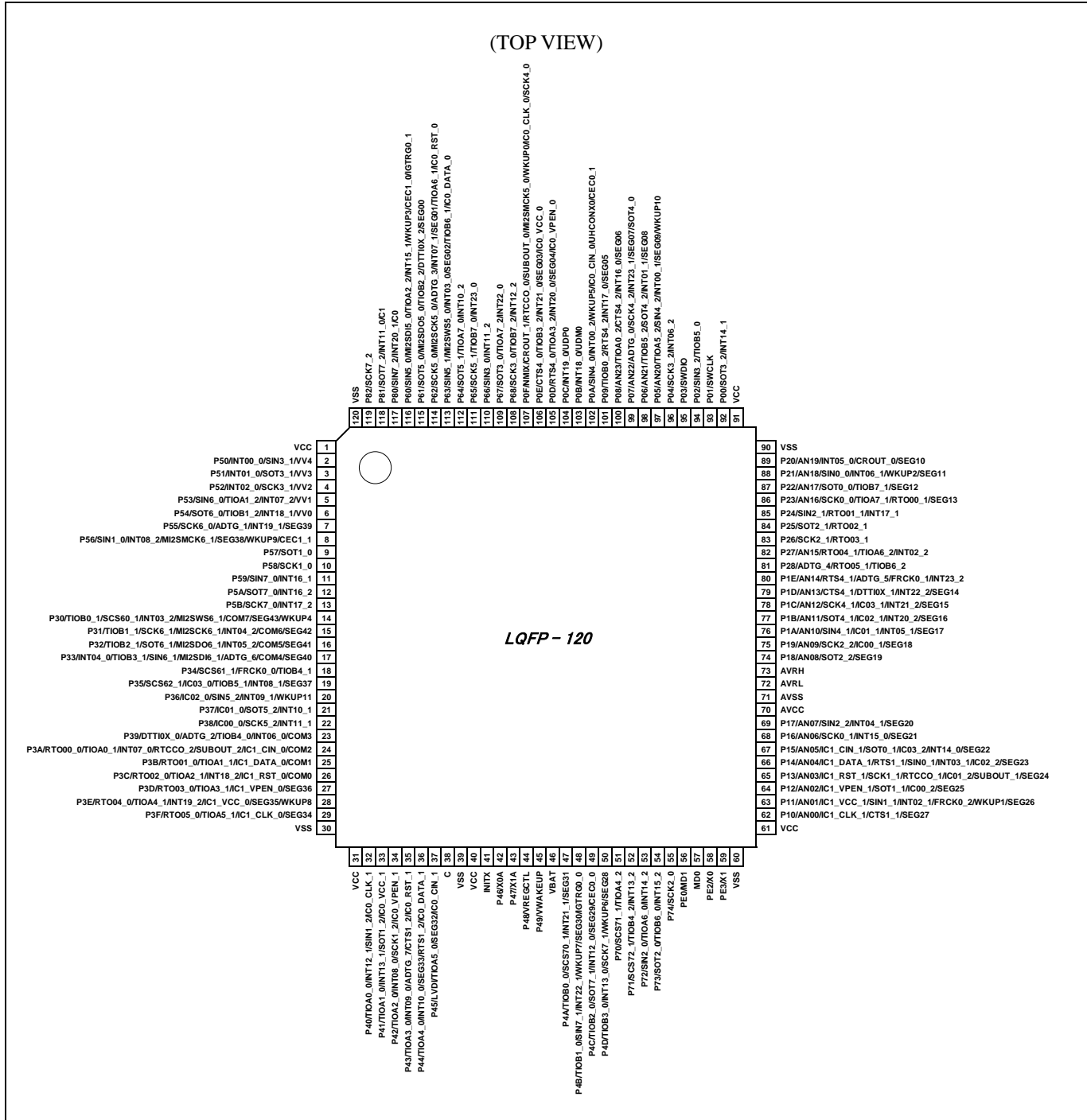
FPT-100P-M20



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

FPT-120P-M21



**Note:**

- The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

#### 4. List of Pin Functions

##### List of Pin Numbers

The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
1	1	1	VCC	-	
2	2	2	P50	Q	X
			SIN3_1		
			INT00_0		
			VV4		
3	3	3	P51	Q	X
			SOT3_1		
			INT01_0		
			VV3		
4	4	4	P52	Q	X
			SCK3_1		
			INT02_0		
			VV2		
5	5	5	P53	Q	X
			SIN6_0		
			TIOA1_2		
			INT07_2		
6	6	6	VV1	Q	X
			P54		
			SOT6_0		
			TIOB1_2		
7	7	7	INT18_1	L	S
			VV0		
			P55		
			SCK6_0		
8	8	8	ADTG_1	L	U
			INT19_1		
			SEG39		
			P56		
			MI2SMCK6_1		
			CEC1_1		
INT08_2					
9	-	-	WKUP9	F	I
			SEG38		
10	-	-	SIN1_0	F	I
			P57		
11	-	-	SOT1_0	F	J
			P58		
11	-	-	SCK1_0	F	J
			P59		
			SIN7_0		
			INT16_1		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
12	-	-	P5A	F	J
			SOT7_0		
			INT16_2		
13	-	-	P5B	F	J
			SCK7_0		
			INT17_2		
14	9	9	P30	M	T
			TIOB0_1		
			SCS60_1		
			MI2SWS6_1		
			INT03_2		
			WKUP4		
			COM7		
SEG43					
15	10	10	P31	M	S
			TIOB1_1		
			SCK6_1		
			MI2SCK6_1		
			INT04_2		
			COM6		
SEG42					
16	11	11	P32	M	S
			TIOB2_1		
			SOT6_1		
			MI2SDO6_1		
			INT05_2		
			COM5		
SEG41					
17	12	12	P33	M	S
			TIOB3_1		
			SIN6_1		
			MI2SDI6_1		
			INT04_0		
			ADTG_6		
			COM4		
SEG40					
18	13	-	P34	I	I
			SCS61_1		
			FRCK0_0		
19	14	-	TIOB4_1	L	S
			P35		
			SCS62_1		
			IC03_0		
			TIOB5_1		
INT08_1					
SEG37					
20	15	-	P36	I	N
			IC02_0		
			SIN5_2		
			INT09_1		
WKUP11					
21	16	-	P37	I	J
			IC01_0		
			SOT5_2		
			INT10_1		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
22	17	-	P38	F	J
			IC00_0		
			SCK5_2		
			INT11_1		
23	18	13	P39	N	S
			DTTIOX_0		
			TIOB4_0		
			ADTG_2		
			INT06_0		
COM3					
24	19	14	P3A	N	S
			RTO00_0		
			TIOA0_1		
			RTCCO_2		
			SUBOUT_2		
			IC1_CIN_0		
			INT07_0		
COM2					
25	20	15	P3B	N	P
			RTO01_0		
			TIOA1_1		
			IC1_DATA_0		
COM1					
26	21	16	P3C	N	S
			RTO02_0		
			TIOA2_1		
			INT18_2		
			IC1_RST_0		
COM0					
27	22	17	P3D	L	P
			RTO03_0		
			TIOA3_1		
			IC1_VPEN_0		
SEG36					
28	23	18	P3E	L	T
			RTO04_0		
			TIOA4_1		
			IC1_VCC_0		
			INT19_2		
			WKUP8		
SEG35					
29	24	19	P3F	L	P
			RTO05_0		
			TIOA5_1		
			IC1_CLK_0		
SEG34					
30	25	20	VSS	-	-
31	26	-	VCC	-	-
32	27	-	P40	F	J
			TIOA0_0		
			IC0_CLK_1		
			INT12_1		
			SIN1_2		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
33	28	-	P41	F	J
			TIOA1_0		
			SOT1_2		
			IC0_VCC_1		
			INT13_1		
34	29	-	P42	F	J
			TIOA2_0		
			SCK1_2		
			IC0_VPEN_1		
			INT08_0		
35	30	-	P43	F	J
			TIOA3_0		
			CTS1_2		
			ADTG_7		
			IC0_RST_1		
36	31	21	P44	L	S
			TIOA4_0		
			IC0_DATA_1		
			INT10_0		
			RTS1_2		
37	32	22	SEG33	L	P
			P45		
			TIOA5_0		
			IC0_CIN_1		
			LVDI		
38	33	23	SEG32	-	-
39	34	24	C	-	-
40	35	25	VSS	-	-
41	36	26	VCC	-	-
42	37	27	INITX	B	C
43	38	28	P46	D	E
			X0A		
44	39	29	P47	E	F
			X1A		
45	40	30	P48	I	I
			VREGCTL		
46	41	31	P49	I	I
			VWAKEUP		
47	42	32	VBAT	-	-
			P4A		
			TIOB0_0		
			SCS70_1		
			INT21_1		
48	43	33	SEG31	L	T
			P4B		
			TIOB1_0		
			SIN7_1		
			INT22_1		
			WKUP7		
SEG30					
			IGTRG0_0		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
49	44	34	P4C	L	R
			TIOB2_0		
			SOT7_1		
			CEC0_0		
			INT12_0		
50	45	35	SEG29	L	T
			P4D		
			TIOB3_0		
			SCK7_1		
			INT13_0		
51	-	-	WKUP6	F	I
			SEG28		
			P70		
52	-	-	TIOA4_2	F	J
			SCS71_1		
			P71		
53	-	-	TIOB4_2	F	J
			SCS72_1		
			INT13_2		
54	-	-	INT14_2	F	J
			P72		
			SIN2_0		
55	-	-	TIOA6_0	F	I
			INT15_2		
			P73		
56	46	36	SOT2_0	F	J
			TIOB6_0		
			INT15_2		
57	47	37	P74	F	I
			SCK2_0		
58	48	38	PE0	C	D
			MD1		
59	49	39	MD0	J	M
60	50	40	PE2	A	A
			X0		
61	51	41	PE3	A	B
			X1		
62	52	42	VSS	-	-
63	53	43	VCC	P	K
			P10		
			IC1_CLK_1		
			CTS1_1		
			AN00		
63	53	43	SEG27	P	W
			P11		
			IC1_VCC_1		
			SIN1_1		
			FRCK0_2		
			INT02_1		
			WKUP1		
AN01					
SEG26					



Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
64	54	44	P12	P	K
			IC1_VPEN_1		
			SOT1_1		
			IC00_2		
			AN02		
65	55	45	SEG25	P	K
			P13		
			IC1_RST_1		
			SCK1_1		
			RTCCO_1		
			IC01_2		
66	56	46	SUBOUT_1	P	V
			AN03		
			SEG24		
			P14		
			IC1_DATA_1		
			RTS1_1		
67	57	47	SIN0_1	P	V
			IC02_2		
			INT03_1		
			AN04		
			SEG23		
			P15		
68	58	48	IC1_CIN_1	P	V
			SOT0_1		
			IC03_2		
			INT14_0		
			AN05		
			SEG22		
69	59	49	P16	P	V
			SCK0_1		
			INT15_0		
			AN06		
70	60	50	SEG21	-	-
			P17		
			SIN2_2		
			INT04_1		
71	61	51	AN07	-	-
			SEG20		
			AVCC		
72	62	52	AVSS	-	-
			AVRL		
73	63	53	AVRH	-	-
74	64	54	P18	P	K
			SOT2_2		
			AN08		
			SEG19		
75	65	55	P19	P	K
			SCK2_2		
			IC00_1		
			AN09		
			SEG18		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
76	66	56	P1A	P	V
			SIN4_1		
			IC01_1		
			INT05_1		
			AN10		
			SEG17		
77	67	57	P1B	P	V
			SOT4_1		
			IC02_1		
			INT20_2		
			AN11		
			SEG16		
78	68	-	P1C	P	V
			SCK4_1		
			IC03_1		
			INT21_2		
			AN12		
			SEG15		
79	69	-	P1D	P	V
			CTS4_1		
			DTTI0X_1		
			INT22_2		
			AN13		
			SEG14		
80	70	-	P1E	H	L
			RTS4_1		
			FRCK0_1		
			ADTG_5		
			INT23_2		
			AN14		
81	-	-	P28	F	I
			RTO05_1		
			TIOB6_2		
			ADTG_4		
82	-	-	P27	G	L
			RTO04_1		
			TIOA6_2		
			INT02_2		
			AN15		
83	-	-	P26	F	I
			SCK2_1		
			RTO03_1		
84	-	-	P25	F	I
			SOT2_1		
			RTO02_1		
85	-	-	P24	F	J
			SIN2_1		
			RTO01_1		
			INT17_1		
86	71	58	P23	P	K
			SCK0_0		
			TIOA7_1		
			RTO00_1		
			AN16		
			SEG13		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
87	72	59	P22	P	K
			SOT0_0		
			TIOB7_1		
			AN17		
88	73	60	SEG12	P	W
			P21		
			SIN0_0		
			INT06_1		
89	74	-	WKUP2	P	V
			AN18		
			SEG11		
			P20		
90	75	-	INT05_0	-	-
91	76	-	CROUT_0	-	-
92	77	61	AN19	I	J
			SEG10		
			VSS		
93	78	62	VCC	I	H
			P00		
			SOT3_2		
94	79	63	INT14_1	I	I
			P01		
			SWCLK		
95	80	64	P02	I	H
			SIN3_2		
			TIOB5_0		
96	81	65	P03	I	J
			SWDIO		
			P04		
97	82	-	SCK3_2	P	W
			INT06_2		
			P05		
			TIOA5_2		
			SIN4_2		
			INT00_1		
98	83	-	WKUP10	P	V
99	84	66	AN20		
			SEG09		
			P06		
			TIOB5_2		
			SOT4_2		
INT01_1	P	V			
AN21					
SEG08					
P07					
SCK4_2					
ADTG_0					
99	84	66	INT23_1	P	V
			AN22		
			SEG07		
			SOT4_0		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
100	85	-	P08	P	V
			TIOA0_2		
			CTS4_2		
			INT16_0		
			AN23		
			SEG06		
101	86	-	P09	L	S
			TIOB0_2		
			RTS4_2		
			INT17_0		
102	87	67	SEG05	I	O
			P0A		
			SIN4_0		
			INT00_2		
			WKUP5		
			IC0_CIN_0		
103	88	68	UHC0N0	K	Q
			CEC0_1		
			P0B		
104	89	69	INT18_0	K	Q
			UDM0		
			P0C		
105	90	70	INT19_0	L	S
			UDP0		
			P0D		
			RTS4_0		
			TIOA3_2		
106	91	71	INT20_0	L	S
			SEG04		
			IC0_VPEN_0		
			P0E		
			CTS4_0		
107	92	72	TIOB3_2	I	G
			INT21_0		
			SEG03		
			IC0_VCC_0		
			P0F		
			CROUT_1		
			RTCCO_0		
			SUBOUT_0		
MI2SMCK5_0					
108	-	-	NMIX	F	J
			WKUP0		
			IC0_CLK_0		
			SCK4_0		
109	-	-	P68	F	J
			SCK3_0		
			TIOB7_2		
			INT12_2		
110	-	-	P67	F	J
			SOT3_0		
			TIOA7_2		
			INT22_0	F	J
			P66		
			SIN3_0		
			INT11_2		

Pin No.			Pin Name	I/O Circuit Type	Pin State Type
LQFP-120	LQFP-100	LQFP-80			
111	-	-	P65	F	J
			SCK5_1		
			TIOB7_0		
			INT23_0		
112	-	-	P64	F	J
			SOT5_1		
			TIOA7_0		
			INT10_2		
113	93	73	P63	L	S
			MI2SWS5_0		
			INT03_0		
	SEG02				
	TIOB6_1				
	IC0_DATA_0				
-	-	SIN5_1			
114	94	74	P62	L	S
			SCK5_0		
			MI2SCK5_0		
			ADTG_3		
			INT07_1		
			SEG01		
			TIOA6_1		
IC0_RST_0					
115	95	75	P61	L	P
			SOT5_0		
			MI2SDO5_0		
			TIOB2_2		
			DTTIOX_2		
SEG00					
116	96	76	P60	I	O
			SIN5_0		
			MI2SDI5_0		
			TIOA2_2		
			CEC1_0		
			INT15_1		
			WKUP3		
IGTRG0_1					
117	97	77	P80	O	J
			SIN7_2		
			INT20_1		
118	98	78	C0	O	J
			P81		
			SOT7_2		
			INT11_0		
119	99	79	C1	I	I
			P82		
120	100	80	SCK7_2	-	-
			VSS	-	-

\*: 5 V tolerant I/O

**List of Pin Functions**

The number after the underscore ("\_") in a pin name such as XXX\_1 and XXX\_2 indicates the relocated port number. The channel on such pin has multiple functions, each of which has its own pin name. Use the Extended Port Function Register (EPFR) to select the pin to be used.

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
ADC	ADTG_0	A/D converter external trigger input pin	99	84	66
	ADTG_1		7	7	7
	ADTG_2		23	18	13
	ADTG_3		114	94	74
	ADTG_4		81	-	-
	ADTG_5		80	70	-
	ADTG_6		17	12	12
	ADTG_7		35	30	-
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	62	52	42
	AN01		63	53	43
	AN02		64	54	44
	AN03		65	55	45
	AN04		66	56	46
	AN05		67	57	47
	AN06		68	58	48
	AN07		69	59	49
	AN08		74	64	54
	AN09		75	65	55
	AN10		76	66	56
	AN11		77	67	57
	AN12		78	68	-
	AN13		79	69	-
	AN14		80	70	-
	AN15		82	-	-
	AN16		86	71	58
	AN17		87	72	59
	AN18		88	73	60
	AN19		89	74	-
	AN20		97	82	-
	AN21		98	83	-
AN22	99		84	66	
AN23	100	85	-		
Base Timer 0	TIOA0_0	Base timer ch.0 TIOA pin	32	27	-
	TIOA0_1		24	19	14
	TIOA0_2		100	85	-
	TIOB0_0	Base timer ch.0 TIOB pin	47	42	32
	TIOB0_1		14	9	9
	TIOB0_2		101	86	-

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Base Timer 1	TIOA1_0	Base timer ch.1 TIOA pin	33	28	-
	TIOA1_1		25	20	15
	TIOA1_2		5	5	5
	TIOB1_0	Base timer ch.1 TIOB pin	48	43	33
	TIOB1_1		15	10	10
	TIOB1_2		6	6	6
Base Timer 2	TIOA2_0	Base timer ch.2 TIOA pin	34	29	-
	TIOA2_1		26	21	16
	TIOA2_2		116	96	76
	TIOB2_0	Base timer ch.2 TIOB pin	49	44	34
	TIOB2_1		16	11	11
	TIOB2_2		115	95	75
Base Timer 3	TIOA3_0	Base timer ch.3 TIOA pin	35	30	-
	TIOA3_1		27	22	17
	TIOA3_2		105	90	70
	TIOB3_0	Base timer ch.3 TIOB pin	50	45	35
	TIOB3_1		17	12	12
	TIOB3_2		106	91	71
Base Timer 4	TIOA4_0	Base timer ch.4 TIOA pin	36	31	21
	TIOA4_1		28	23	18
	TIOA4_2		51	-	-
	TIOB4_0	Base timer ch.4 TIOB pin	23	18	13
	TIOB4_1		18	13	-
	TIOB4_2		52	-	-
Base Timer 5	TIOA5_0	Base timer ch.5 TIOA pin	37	32	22
	TIOA5_1		29	24	19
	TIOA5_2		97	82	-
	TIOB5_0	Base timer ch.5 TIOB pin	94	79	63
	TIOB5_1		19	14	-
	TIOB5_2		98	83	-
Base Timer 6	TIOA6_0	Base timer ch.6 TIOA pin	53	-	-
	TIOA6_1		114	94	74
	TIOA6_2		82	-	-
	TIOB6_0	Base timer ch.6 TIOB pin	54	-	-
	TIOB6_1		113	93	73
	TIOB6_2		81	-	-
Base Timer 7	TIOA7_0	Base timer ch.7 TIOA pin	112	-	-
	TIOA7_1		86	71	58
	TIOA7_2		109	-	-
	TIOB7_0	Base timer ch.7 TIOB pin	111	-	-
	TIOB7_1		87	72	59
	TIOB7_2		108	-	-
Debugger	SWCLK	Serial wire debug interface clock input pin	93	78	62
	SWDIO	Serial wire debug interface data input / output pin	95	80	64

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT00_0	External interrupt request 00 input pin	2	2	2
	INT00_1		97	82	-
	INT00_2		102	87	67
	INT01_0	External interrupt request 01 input pin	3	3	3
	INT01_1		98	83	-
	INT02_0	External interrupt request 02 input pin	4	4	4
	INT02_1		63	53	43
	INT02_2		82	-	-
	INT03_0	External interrupt request 03 input pin	113	93	73
	INT03_1		66	56	46
	INT03_2		14	9	9
	INT04_0	External interrupt request 04 input pin	17	12	12
	INT04_1		69	59	49
	INT04_2		15	10	10
	INT05_0	External interrupt request 05 input pin	89	74	-
	INT05_1		76	66	56
	INT05_2		16	11	11
	INT06_0	External interrupt request 06 input pin	23	18	13
	INT06_1		88	73	60
	INT06_2		96	81	65
	INT07_0	External interrupt request 07 input pin	24	19	14
	INT07_1		114	94	74
	INT07_2		5	5	5
	INT08_0	External interrupt request 08 input pin	34	29	-
	INT08_1		19	14	-
	INT08_2		8	8	8
	INT09_0	External interrupt request 09 input pin	35	30	-
	INT09_1		20	15	-
	INT10_0	External interrupt request 10 input pin	36	31	21
	INT10_1		21	16	-
INT10_2	112		-	-	
INT11_0	External interrupt request 11 input pin	118	98	78	
INT11_1		22	17	-	
INT11_2		110	-	-	
INT12_0	External interrupt request 12 input pin	49	44	34	
INT12_1		32	27	-	
INT12_2		108	-	-	
INT13_0	External interrupt request 13 input pin	50	45	35	
INT13_1		33	28	-	
INT13_2		52	-	-	
INT14_0	External interrupt request 14 input pin	67	57	47	
INT14_1		92	77	61	
INT14_2		53	-	-	



Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
External Interrupt	INT15_0	External interrupt request 15 input pin	68	58	48
	INT15_1		116	96	76
	INT15_2		54	-	-
	INT16_0	External interrupt request 16 input pin	100	85	-
	INT16_1		11	-	-
	INT16_2		12	-	-
	INT17_0	External interrupt request 17 input pin	101	86	-
	INT17_1		85	-	-
	INT17_2		13	-	-
	INT18_0	External interrupt request 18 input pin	103	88	68
	INT18_1		6	6	6
	INT18_2		26	21	16
	INT19_0	External interrupt request 19 input pin	104	89	69
	INT19_1		7	7	7
	INT19_2		28	23	18
	INT20_0	External interrupt request 20 input pin	105	90	70
	INT20_1		117	97	77
	INT20_2		77	67	57
	INT21_0	External interrupt request 21 input pin	106	91	71
	INT21_1		47	42	32
	INT21_2		78	68	-
	INT22_0	External interrupt request 22 input pin	109	-	-
	INT22_1		48	43	33
INT22_2	79		69	-	
INT23_0	External interrupt request 23 input pin	111	-	-	
INT23_1		99	84	66	
INT23_2		80	70	-	
	NMIX	Non-Maskable Interrupt input pin	107	92	72
GPIO	P00	General-purpose I/O port 0	92	77	61
	P01		93	78	62
	P02		94	79	63
	P03		95	80	64
	P04		96	81	65
	P05		97	82	-
	P06		98	83	-
	P07		99	84	66
	P08		100	85	-
	P09		101	86	-
	P0A		102	87	67
	P0B		103	88	68
	P0C		104	89	69
	P0D		105	90	70
	P0E		106	91	71
P0F	107	92	72		

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
GPIO	P10	General-purpose I/O port 1	62	52	42
	P11		63	53	43
	P12		64	54	44
	P13		65	55	45
	P14		66	56	46
	P15		67	57	47
	P16		68	58	48
	P17		69	59	49
	P18		74	64	54
	P19		75	65	55
	P1A		76	66	56
	P1B		77	67	57
	P1C		78	68	-
	P1D		79	69	-
	P1E		80	70	-
	P20	General-purpose I/O port 2	89	74	-
	P21		88	73	60
	P22		87	72	59
	P23		86	71	58
	P24		85	-	-
	P25		84	-	-
	P26		83	-	-
	P27		82	-	-
	P28		81	-	-
	P30		General-purpose I/O port 3	14	9
	P31	15		10	10
	P32	16		11	11
	P33	17		12	12
	P34	18		13	-
	P35	19		14	-
	P36	20		15	-
	P37	21		16	-
	P38	22		17	-
P39	23	18		13	
P3A	24	19		14	
P3B	25	20		15	
P3C	26	21	16		
P3D	27	22	17		
P3E	28	23	18		
P3F	29	24	19		

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
GPIO	P40	General-purpose I/O port 4	32	27	-
	P41		33	28	-
	P42		34	29	-
	P43		35	30	-
	P44		36	31	21
	P45		37	32	22
	P46		42	37	27
	P47		43	38	28
	P48		44	39	29
	P49		45	40	30
	P4A		47	42	32
	P4B		48	43	33
	P4C		49	44	34
	P4D		50	45	35
	P50	General-purpose I/O port 5	2	2	2
	P51		3	3	3
	P52		4	4	4
	P53		5	5	5
	P54		6	6	6
	P55		7	7	7
	P56		8	8	8
	P57		9	-	-
	P58		10	-	-
	P59		11	-	-
	P5A	12	-	-	
	P5B	13	-	-	
	P60	General-purpose I/O port 6	116	96	76
	P61		115	95	75
	P62		114	94	74
	P63		113	93	73
	P64		112	-	-
	P65		111	-	-
	P66		110	-	-
	P67		109	-	-
	P68	108	-	-	
	P70	General-purpose I/O port 7	51	-	-
P71	52		-	-	
P72	53		-	-	
P73	54		-	-	
P74	55	-	-		
P80	General-purpose I/O port 8	117	97	77	
P81		118	98	78	
P82		119	99	79	
PE0*	General-purpose I/O port E	56	46	36	
PE2		58	48	38	
PE3		59	49	39	

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	88	73	60
	SIN0_1		66	56	46
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin. This pin operates as SOT0 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA0 when used as an I <sup>2</sup> C pin (operation mode 4).	87	72	59
	SOT0_1 (SDA0_1)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I <sup>2</sup> C pin (operation mode 4).	67	57	47
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I <sup>2</sup> C pin (operation mode 4).	86	71	58
	SCK0_1 (SCL0_1)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when used as a CSIO pin (operation mode 2) and as SCL0 when used as an I <sup>2</sup> C pin (operation mode 4).	68	58	48
Multi-function Serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	8	-	-
	SIN1_1		63	53	43
	SIN1_2		32	27	-
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I <sup>2</sup> C pin (operation mode 4).	9	-	-
	SOT1_1 (SDA1_1)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I <sup>2</sup> C pin (operation mode 4).	64	54	44
	SOT1_2 (SDA1_2)	Multi-function serial interface ch.1 output pin. This pin operates as SOT1 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA1 when used as an I <sup>2</sup> C pin (operation mode 4).	33	28	-
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I <sup>2</sup> C pin (operation mode 4).	10	-	-
	SCK1_1 (SCL1_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I <sup>2</sup> C pin (operation mode 4).	65	55	45
	SCK1_2 (SCL1_2)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when used as a CSIO pin (operation mode 2) and as SCL1 when used as an I <sup>2</sup> C pin (operation mode 4).	34	29	-
Multi-function Serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	53	-	-
	SIN2_1		85	-	-
	SIN2_2		69	59	49
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA2 when used as an I <sup>2</sup> C pin (operation mode 4).	54	-	-
	SOT2_1 (SDA2_1)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA2 when used as an I <sup>2</sup> C pin (operation mode 4).	84	-	-
	SOT2_2 (SDA2_2)	Multi-function serial interface ch.2 output pin. This pin operates as SOT2 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA2 when used as an I <sup>2</sup> C pin (operation mode 4).	74	64	54
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK2 when used as a CSIO pin (operation mode 2) and as SCL2 when used as an I <sup>2</sup> C pin (operation mode 4).	55	-	-
	SCK2_1 (SCL2_1)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK2 when used as a CSIO pin (operation mode 2) and as SCL2 when used as an I <sup>2</sup> C pin (operation mode 4).	83	-	-
	SCK2_2 (SCL2_2)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK2 when used as a CSIO pin (operation mode 2) and as SCL2 when used as an I <sup>2</sup> C pin (operation mode 4).	75	65	55

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 3	SIN3_0	Multi-function serial interface ch.3 input pin	110	-	-
	SIN3_1		2	2	2
	SIN3_2		94	79	63
	SOT3_0 (SDA3_0)	Multi-function serial interface ch.3 output pin.	109	-	-
	SOT3_1 (SDA3_1)	This pin operates as SOT3 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA3 when used as an I <sup>2</sup> C pin (operation mode 4).	3	3	3
	SOT3_2 (SDA3_2)		92	77	61
	SCK3_0 (SCL3_0)	Multi-function serial interface ch.3 clock I/O pin.	108	-	-
	SCK3_1 (SCL3_1)	This pin operates as SCK3 when used as a CSIO (operation mode 2) and as SCL3 when used as an I <sup>2</sup> C pin (operation mode 4).	4	4	4
	SCK3_2 (SCL3_2)		96	81	65
Multi-function Serial 4	SIN4_0	Multi-function serial interface ch.4 input pin	102	87	67
	SIN4_1		76	66	56
	SIN4_2		97	82	-
	SOT4_0 (SDA4_0)	Multi-function serial interface ch.4 output pin.	99	84	66
	SOT4_1 (SDA4_1)	This pin operates as SOT4 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA4 when used as an I <sup>2</sup> C pin (operation mode 4).	77	67	57
	SOT4_2 (SDA4_2)		98	83	-
	SCK4_0 (SCL4_0)	Multi-function serial interface ch.4 clock I/O pin.	107	92	72
	SCK4_1 (SCL4_1)	This pin operates as SCK4 when used as a CSIO (operation mode 2) and as SCL4 when used as an I <sup>2</sup> C pin (operation mode 4).	78	68	-
	SCK4_2 (SCL4_2)		99	84	66
	CTS4_0	Multi-function serial interface ch4 CTS input pin	106	91	71
	CTS4_1		79	69	-
	CTS4_2		100	85	-
	RTS4_0	Multi-function serial interface ch4 RTS input pin	105	90	70
	RTS4_1		80	70	-
RTS4_2	101		86	-	

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 5	SIN5_0 (MI2SDI5_0)	Multi-function serial interface ch.5 input pin. SIN5_0 pin operates as I2SIN5_0 when used as an I <sup>2</sup> S pin (operation mode 2).	116	96	76
	SIN5_1		113	-	-
	SIN5_2		20	15	-
	SOT5_0 (SDA5_0) (MI2SDO5_0)	Multi-function serial interface ch.5 output pin. This pin operates as SOT5 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA5 when used as an I <sup>2</sup> C pin (operation mode 4). SOT5_0 pin operates as MI2SDO5_0 when used as an I <sup>2</sup> S pin (operation mode 2).	115	95	75
	SOT5_1 (SDA5_1)		112	-	-
	SOT5_2 (SDA5_2)		21	16	-
	SCK5_0 (SCL5_0) (MI2SCK5_0)	Multi-function serial interface ch.5 clock I/O pin. This pin operates as SCK5 when used as a CSIO (operation mode 2) and as SCL5 when used as an I <sup>2</sup> C pin (operation mode 4). SCK5_0 pin operates as MI2SCK5_0 when used as an I <sup>2</sup> S pin (operation mode 2).	114	94	74
	SCK5_1 (SCL5_1)		111	-	-
	SCK5_2 (SCL5_2)		22	17	-
MI2SWS5_0	I <sup>2</sup> S word select (WS) output	113	93	73	
Multi-function Serial 6	SIN6_0	Multi-function serial interface ch.6 input pin. SIN6_1 pin operates as I2SIN6_1 when used as an I <sup>2</sup> S pin (operation mode 2).	5	5	5
	SIN6_1 (MI2SDI6_1)		17	12	12
	SOT6_0 (SDA6_0)	Multi-function serial interface ch.6 output pin. This pin operates as SOT6 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA6 when used as an I <sup>2</sup> C pin (operation mode 4). SOT6_1 pin operates as MI2SDO6_1 when used as an I <sup>2</sup> S pin (operation mode 2).	6	6	6
	SOT6_1 (SDA6_1) (MI2SDO6_1)		16	11	11
	SCK6_0 (SCL6_0)		7	7	7
	SCK6_1 (SCL6_1) (MI2SCK6_1)	Multi-function serial interface ch.6 clock I/O pin. This pin operates as SCK6 when used as a CSIO (operation mode 2) and as SCL6 when used as an I <sup>2</sup> C pin (operation mode 4). SCK6_6 pin operates as MI2SCK6_1 when used as an I <sup>2</sup> S pin (operation mode 2).	15	10	10
	SCS60_1		14	9	9
	SCS61_1		18	13	-
	SCS62_1	Multi-function serial interface ch.6 serial chip select 2 input/output pin.	19	14	-
MI2SWS6_1	I <sup>2</sup> S word select (WS) output	14	9	9	

Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Multi-function Serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	11	-	-
	SIN7_1		48	43	33
	SIN7_2		117	97	77
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin.	12	-	-
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when used as a UART/CSIO/LIN pin (operation mode 0 to 3) and as SDA7 when used as an I <sup>2</sup> C pin (operation mode 4).	49	44	34
	SOT7_2 (SDA7_2)		118	98	78
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin.	13	-	-
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when used as a CSIO (operation mode 2) and as SCL7 when used as an I <sup>2</sup> C pin (operation mode 4).	50	45	35
	SCK7_2 (SCL7_2)		119	99	79
	SCS70_1	Multi-function serial interface ch.7 serial chip select 0 input/output pin.	47	42	32
	SCS71_1	Multi-function serial interface ch.7 serial chip select 1 input/output pin.	51	-	-
	SCS72_1	Multi-function serial interface ch.7 serial chip select 2 input/output pin.	52	-	-
	Smart Card Interface 0	IC0_VCC_0	Smart card ch.0 power enable output pin	106	91
IC0_VCC_1		33		28	-
IC0_VPEN_0		Smart card ch.0 programming output pin	105	90	70
IC0_VPEN_1			34	29	-
IC0_RST_0		Smart card ch.0 reset output pin	114	94	74
IC0_RST_1			35	30	-
IC0_CIN_0		Smart card ch.0 insert detection input pin	102	87	67
IC0_CIN_1			37	32	22
IC0_CLK_0		Smart card ch.0 serial interface clock output pin	107	92	72
IC0_CLK_1			32	27	-
IC0_DATA_0		Smart card ch.0 serial interface data input/output pin	113	93	73
IC0_DATA_1	36		31	21	
Smart Card Interface 1	IC1_VCC_0	Smart card ch.1 power enable output pin	28	23	18
	IC1_VCC_1		63	53	43
	IC1_VPEN_0	Smart card ch.1 programming output pin	27	22	17
	IC1_VPEN_1		64	54	44
	IC1_RST_0	Smart card ch.1 reset output pin	26	21	16
	IC1_RST_1		65	55	45
	IC1_CIN_0	Smart card ch.1 insert detection input pin	24	19	14
	IC1_CIN_1		67	57	47
	IC1_CLK_0	Smart card ch.1 serial interface clock output pin	29	24	19
	IC1_CLK_1		62	52	42
	IC1_DATA_0	Smart card ch.1 serial interface data input/output pin	25	20	15
IC1_DATA_1	66		56	46	
USB	UDM0	USB device/host D – pin	103	88	68
	UDP0	USB device/host D + pin	104	89	69
	UHCONX0	USB external pull-up control pin	102	87	67

Pin Function	Pin Name	Function Description	Pin No.			
			LQFP-120	LQFP-100	LQFP-80	
Multi-function Timer 0	DTTI0X_0	Input signal of waveform generator controlling RTO00 to RTO05 outputs of Multi-function Timer 0.	23	18	13	
	DTTI0X_1		79	69	-	
	DTTI0X_2		115	95	75	
	FRCK0_0	16-bit free-run timer ch.0 external clock input pin.	18	13	-	
	FRCK0_1		80	70	-	
	FRCK0_2		63	53	43	
	IC00_0	16-bit input capture input pin of Multi-function timer 0. ICxx describes channel number.	22	17	-	
	IC00_1		75	65	55	
	IC00_2		64	54	44	
	IC01_0		21	16	-	
	IC01_1		76	66	56	
	IC01_2		65	55	45	
	IC02_0		20	15	-	
	IC02_1		77	67	57	
	IC02_2		66	56	46	
	IC03_0		19	14	-	
	IC03_1		78	68	-	
	IC03_2		67	57	47	
	RTO00_0 (PPG00_0)		Waveform generator output pin of Multi-function timer 0.	24	19	14
	RTO00_1 (PPG00_1)		This pin operates as PPG00 when it is used in PPG0 output mode.	86	71	58
	RTO01_0 (PPG00_0)		Waveform generator output pin of Multi-function timer 0.	25	20	15
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output mode.	85	-	-	
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0.	26	21	16	
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output mode.	84	-	-	
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-function timer 0.	27	22	17	
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output mode.	83	-	-	
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0.	28	23	18	
	RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output mode.	82	-	-	
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-function timer 0.	29	24	19	
	RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output mode.	81	-	-	
IGTRG0_0	PPG IGBT mode external trigger input pin	48	43	33		
IGTRG0_1		116	96	76		



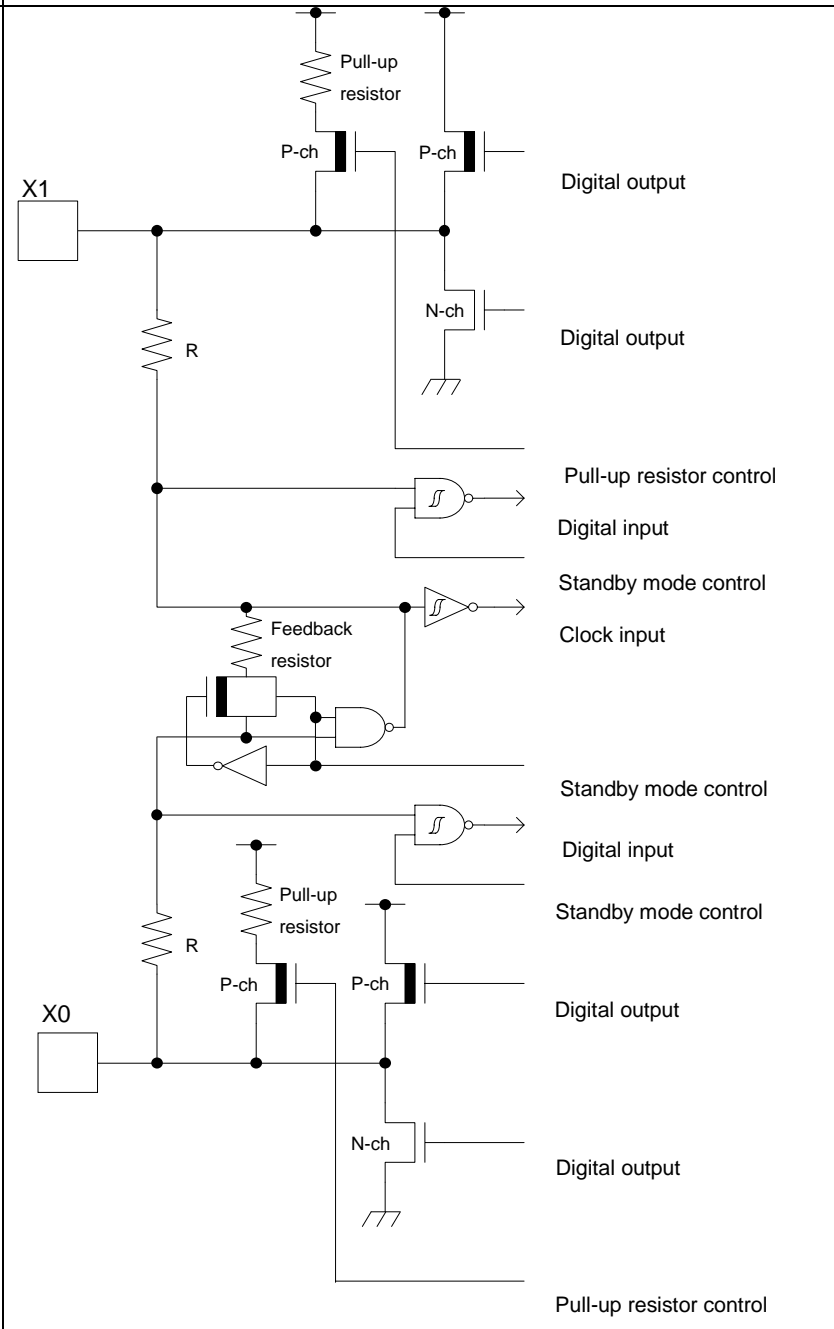
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
Real-time Clock	RTCCO_0	0.5-seconds pulse output pin of Real-time clock	107	92	72
	RTCCO_1		65	55	45
	RTCCO_2		24	19	14
	SUBOUT_0	Sub clock output pin	107	92	72
	SUBOUT_1		65	55	45
	SUBOUT_2		24	19	14
HDMI-CEC/Remote Control Reception	CEC0_0	HDMI-CEC/Remote Control Reception ch.0 input/output pin	49	44	34
	CEC0_1		102	87	67
	CEC1_0	HDMI-CEC/Remote Control Reception ch.1 input/output pin	116	96	76
	CEC1_1		8	8	8
LCD Controller	VV0	LCD controller power supply I/O pin	6	6	6
	VV1		5	5	5
	VV2		4	4	4
	VV3		3	3	3
	VV4		2	2	2
	C0	LCD controller flying capacitor output pin	117	97	77
	C1		118	98	78
	COM0	LCD controller common output pin	26	21	16
	COM1		25	20	15
	COM2		24	19	14
	COM3		23	18	13
	COM4		17	12	12
	COM5		16	11	11
	COM6		15	10	10
	COM7		14	9	9
	SEG00	LCD controller segment output pin	115	95	75
	SEG01		114	94	74
	SEG02		113	93	73
	SEG03		106	91	71
	SEG04		105	90	70
	SEG05		101	86	-
	SEG06		100	85	-
	SEG07		99	84	66
	SEG08		98	83	-
	SEG09		97	82	-
	SEG10		89	74	-
	SEG11		88	73	60
	SEG12		87	72	59
	SEG13		86	71	58
	SEG14		79	69	-
	SEG15		78	68	-
	SEG16		77	67	57

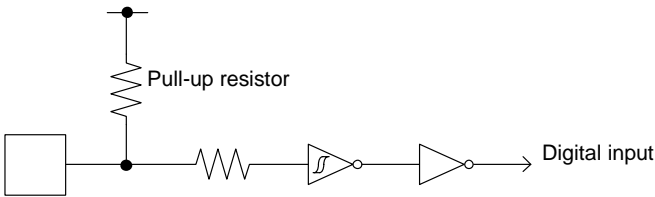
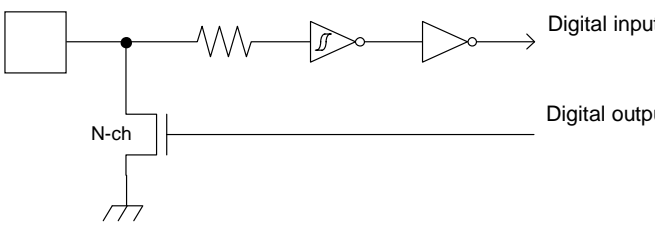
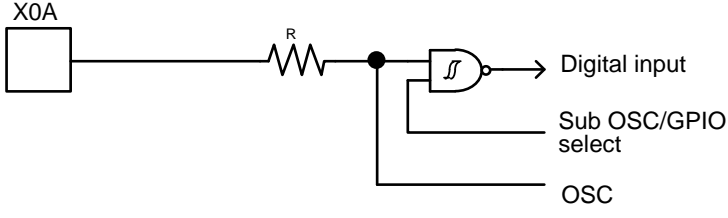
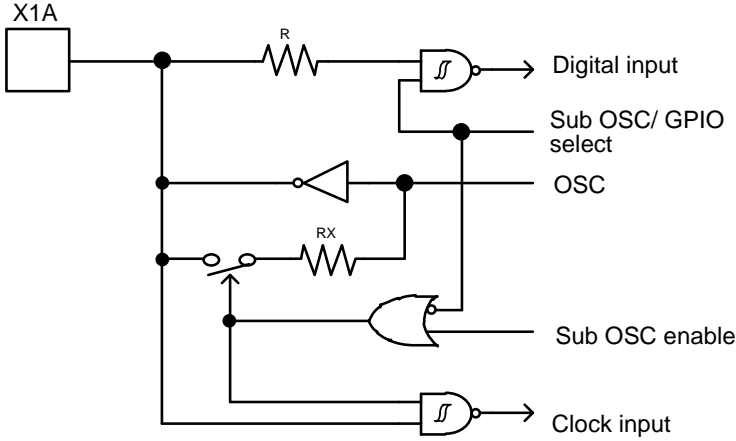
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
LCD Controller	SEG17	LCD controller segment output pin	76	66	56
	SEG18		75	65	55
	SEG19		74	64	54
	SEG20		69	59	49
	SEG21		68	58	48
	SEG22		67	57	47
	SEG23		66	56	46
	SEG24		65	55	45
	SEG25		64	54	44
	SEG26		63	53	43
	SEG27		62	52	42
	SEG28		50	45	35
	SEG29		49	44	34
	SEG30		48	43	33
	SEG31		47	42	32
	SEG32		37	32	22
	SEG33		36	31	21
	SEG34		29	24	19
	SEG35		28	23	18
	SEG36		27	22	17
	SEG37		19	14	-
	SEG38		8	8	8
	SEG39		7	7	7
SEG40	17	12	12		
SEG41	16	11	11		
SEG42	15	10	10		
SEG43	14	9	9		
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin	107	92	72
	WKUP1		63	53	43
	WKUP2		88	73	60
	WKUP3		116	96	76
	WKUP4		14	9	9
	WKUP5		102	87	67
	WKUP6		50	45	35
	WKUP7		48	43	33
	WKUP8		28	23	18
	WKUP9		8	8	8
	WKUP10		97	82	-
	WKUP11		20	15	-

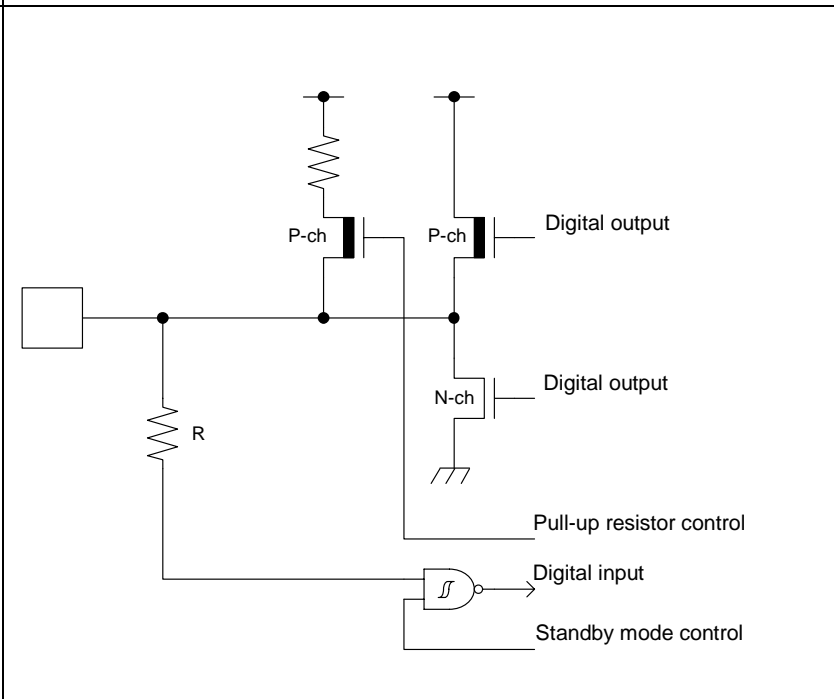
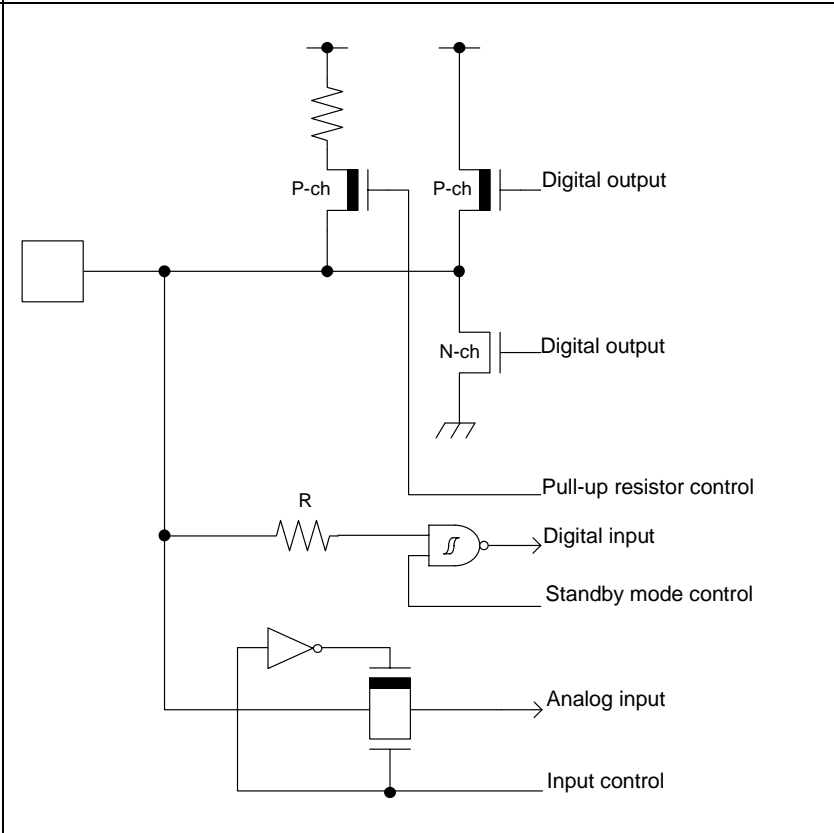
Pin Function	Pin Name	Function Description	Pin No.		
			LQFP-120	LQFP-100	LQFP-80
VBAT	LVDI	Input pin to monitor the external voltage.	37	32	22
	VWAKEUP	The return signal input pin from a hibernation state	45	40	30
	REGCTL	On-board regulator control pin	44	39	29
Reset	INITX	External Reset Input pin. A reset is valid when INITX="L".	41	36	26
Mode	MD0	Mode 0 pin. During normal operation, input MD0="L". During serial programming to Flash memory, input MD0="H".	57	47	37
	MD1	Mode 1 pin. During normal operation, input is not needed. During serial programming to Flash memory, MD1 = "L" must be input.	56	46	36
Power	VCC	Power supply pin	1	1	1
			31	26	-
			40	35	25
			61	51	41
			91	76	-
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	46	41	31
GND	VSS	GND pin	30	25	20
			39	34	24
			60	50	40
			90	75	-
			120	100	80
Clock	X0	Main clock (oscillation) input pin	58	48	38
	X0A	Sub clock (oscillation) input pin	42	37	27
	X1	Main clock (oscillation) I/O pin	59	49	39
	X1A	Sub clock (oscillation) I/O pin	43	38	28
	CROUT_0	Built-in high-speed CR oscillation clock output port	89	74	-
	CROUT_1	Built-in high-speed CR oscillation clock output port	107	92	72
Analog Power	AVCC	A/D converter analog power supply pin	70	60	50
	AVRH	A/D converter analog reference voltage input pin	73	63	53
Analog GND	AVSS	A/D converter analog reference voltage input pin	71	61	51
C pin	C	Power supply stabilization capacitance pin	38	33	23

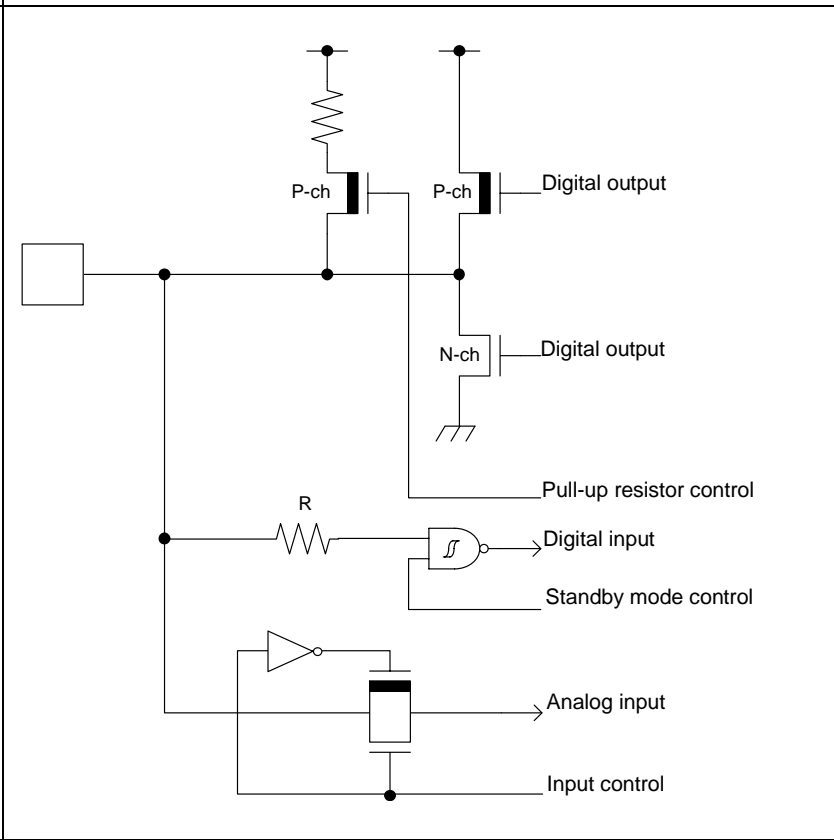
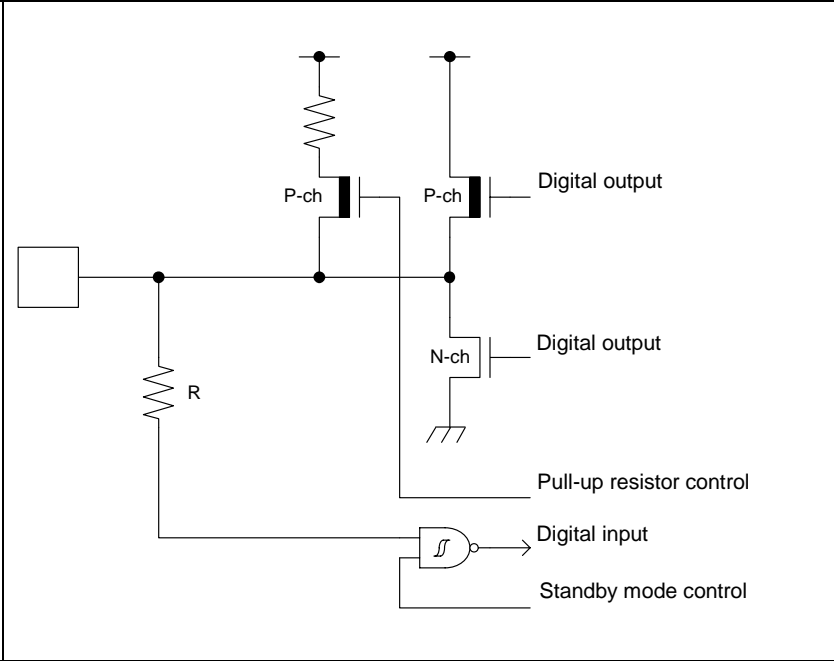
\*: PE0 is an open drain pin, cannot output high.

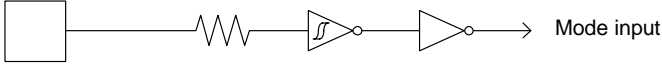
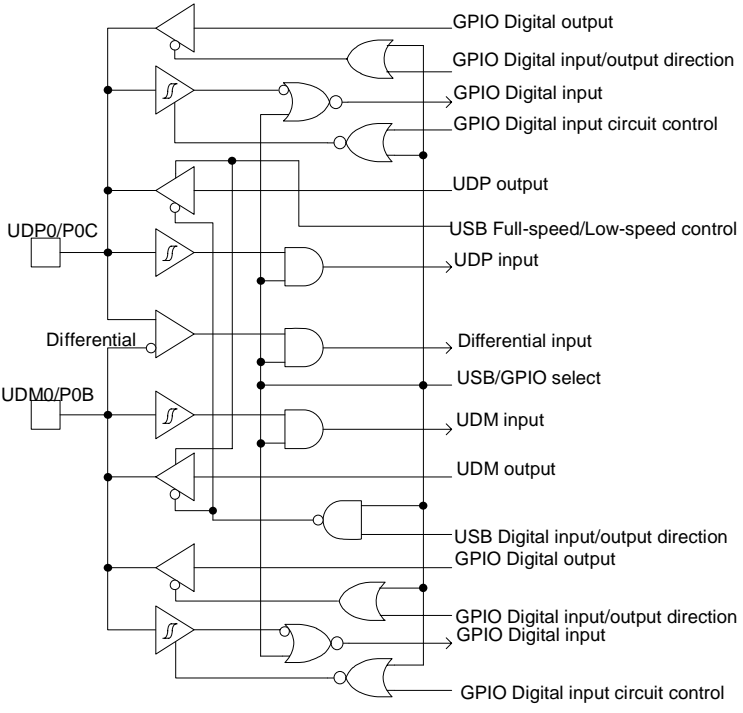
**5. I/O Circuit Type**

Type	Circuit	Remarks
A		<p>It is possible to select the main oscillation / GPIO function</p> <p>When the main oscillation is selected. Oscillation feedback resistor : Approximately 1 MΩ With standby mode control</p> <p>When the GPIO is selected. CMOS level output. CMOS level hysteresis input With pull-up resistor control With standby mode control Pull-up resistor : Approximately 33 kΩ <math>I_{OH} = -4\text{mA}</math>, <math>I_{OL} = 4\text{mA}</math></p>

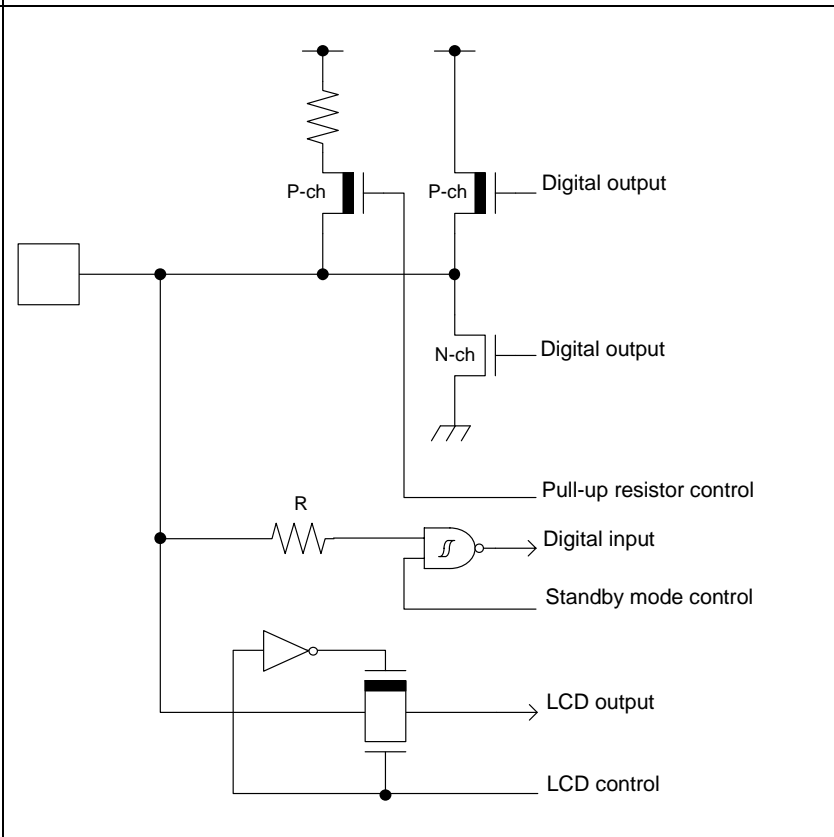
Type	Circuit	Remarks
B		CMOS level hysteresis input Pull-up resistor : Approximately 33 kΩ
C		Open drain output CMOS level hysteresis input
D		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• Please refer to the "VBAT domain" setting of IO in the "Peripheral Manual main part (MN710-00001)".</li> </ul>
E		<p>It is possible to select the sub oscillation / GPIO function</p> <p>When the sub oscillation is selected.</p> <ul style="list-style-type: none"> <li>• Oscillation feedback resistor     : Approximately 12 MΩ</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> </ul> <p>• Please refer to the "VBAT domain" setting of IO in the "Peripheral Manual main part (MN710-00001)" .</p>

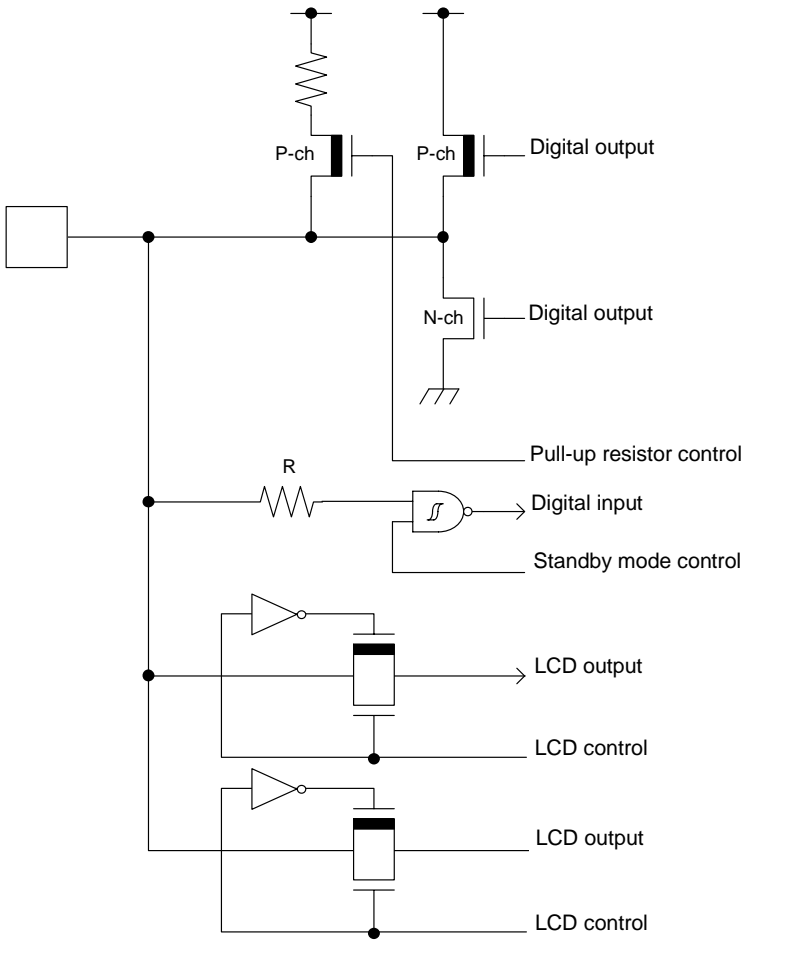
Type	Circuit	Remarks
F		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 k<math>\Omega</math></li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>
G		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 k<math>\Omega</math></li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

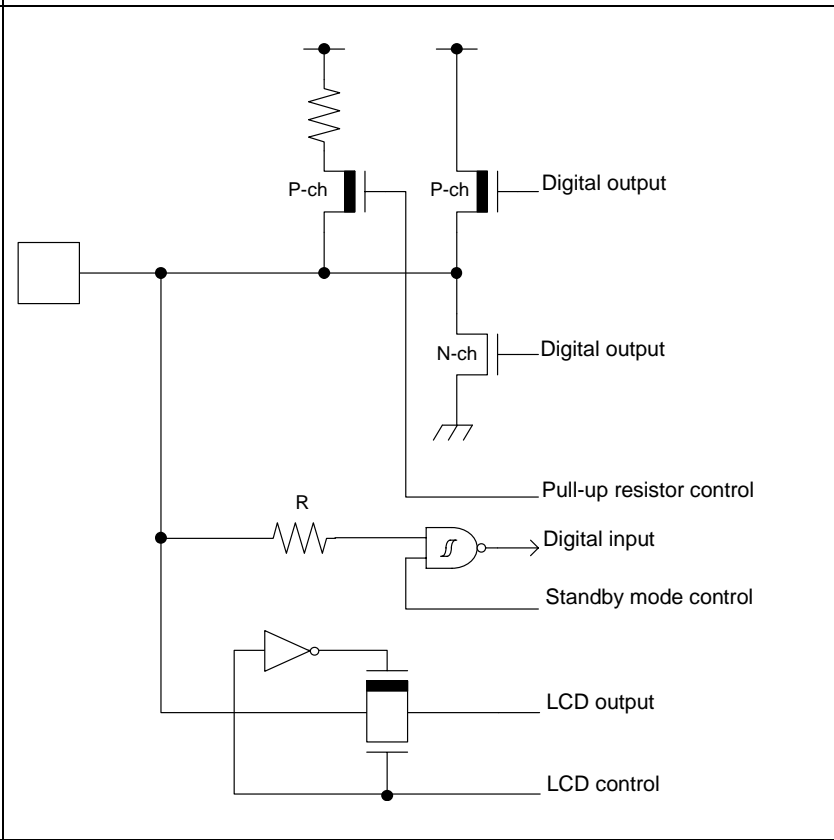
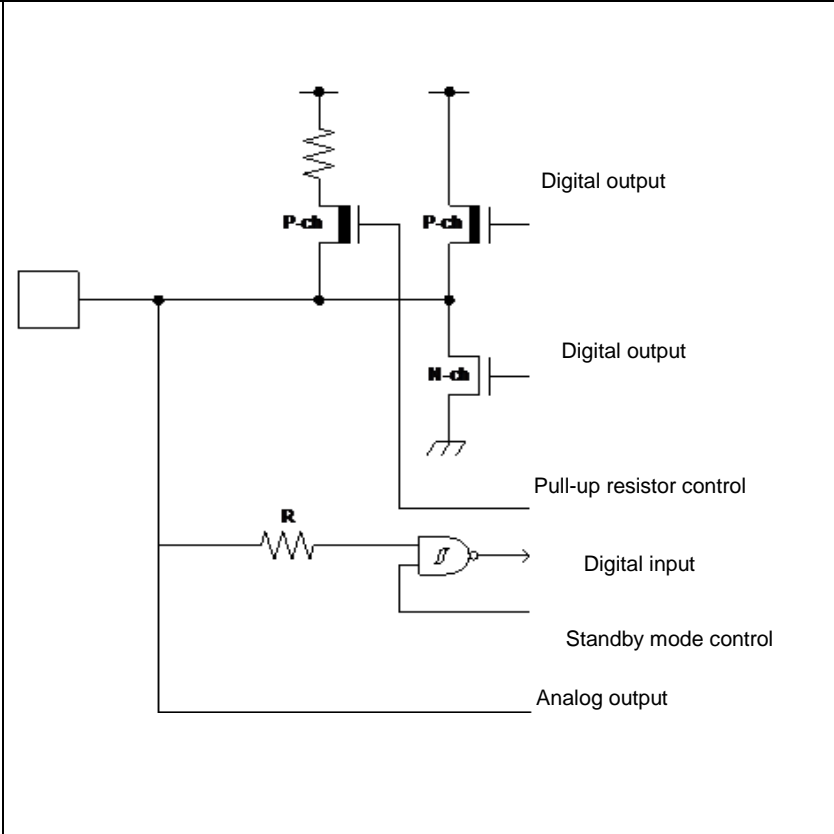
Type	Circuit	Remarks
H		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• 5 V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>
I		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• 5 V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control PZR registers</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

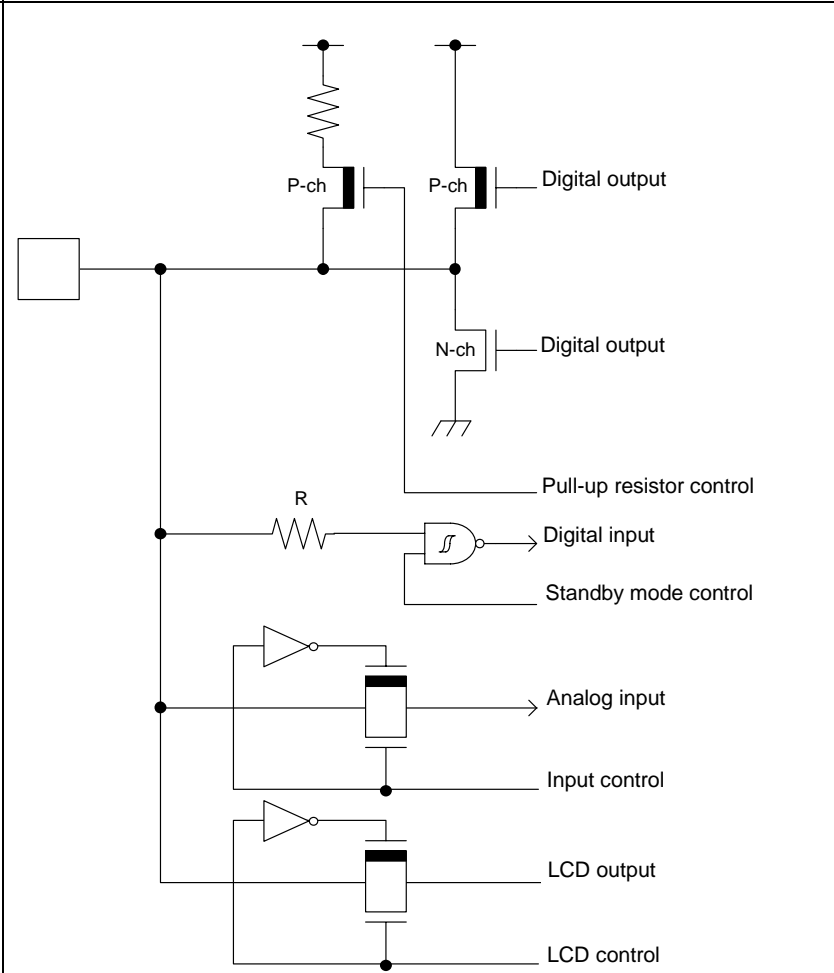
Type	Circuit	Remarks
J		<ul style="list-style-type: none"> <li>• CMOS level hysteresis input</li> </ul>
K		<p>It is possible to select the USB I/O / GPIO function.</p> <p>When the USB I/O is selected.</p> <ul style="list-style-type: none"> <li>• Full-speed, Low-speed control</li> </ul> <p>When the GPIO is selected.</p> <ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With standby mode control</li> </ul>

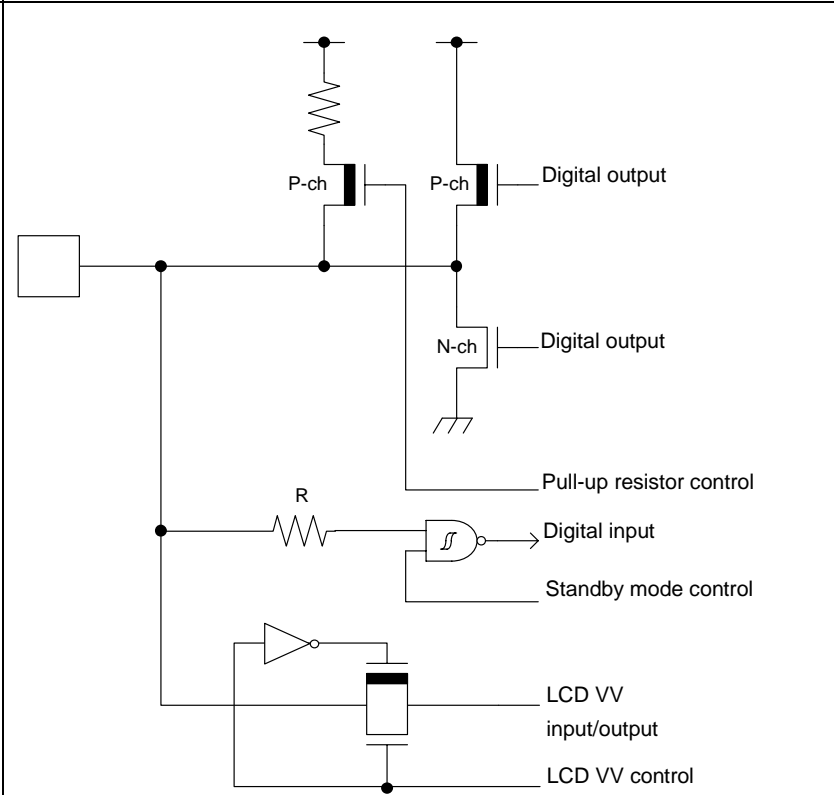


Type	Circuit	Remarks
L		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• 5 V tolerant</li> <li>• LCD segment output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
M	 <p>The circuit diagram for pin M shows a multi-functional output. It features a pull-up resistor connected to a supply rail. The output node is connected to a P-channel MOSFET (P-ch) and an N-channel MOSFET (N-ch). The P-ch MOSFET is labeled 'Digital output'. The N-ch MOSFET is also labeled 'Digital output' and is connected to ground. A pull-up resistor control signal is shown. A digital input is connected through a resistor 'R' to an AND gate, which also receives a standby mode control signal. The AND gate output is labeled 'Digital input'. Two LCD control signals are shown, each driving an LCD output through an inverter and a transistor.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• 5 V tolerant</li> <li>• LCD common output</li> <li>• LCD segment output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
N		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• 5 V tolerant</li> <li>• LCD common output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• Available to control of PZR registers.</li> </ul>
O		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog output</li> <li>• 5 V tolerant</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4</math> mA, <math>I_{OL} = 4</math> mA</li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
P		<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• Analog input</li> <li>• 5 V tolerant</li> <li>• LCD segment output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

Type	Circuit	Remarks
Q	 <p>The circuit diagram for Type Q shows a multiplexer-like structure. It features a central node connected to a pull-up resistor R. This node is controlled by a P-ch transistor (Digital output) and an N-ch transistor (Digital output). A digital input signal, controlled by a standby mode control signal, is connected to the node through a resistor. The node is also connected to an LCD VV input/output and an LCD VV control signal.</p>	<ul style="list-style-type: none"> <li>• CMOS level output</li> <li>• CMOS level hysteresis input</li> <li>• With input control</li> <li>• 5 V tolerant</li> <li>• LCD VV input/output</li> <li>• With pull-up resistor control</li> <li>• With standby mode control</li> <li>• Pull-up resistor : Approximately 33 kΩ</li> <li>• <math>I_{OH} = -4 \text{ mA}</math>, <math>I_{OL} = 4 \text{ mA}</math></li> <li>• Available to control of PZR registers.</li> <li>• When this pin is used as an I<sup>2</sup>C pin, the digital output P-ch transistor is always off</li> </ul>

## 6. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Spansion semiconductor devices.

### 6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

#### Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

#### Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

#### Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

##### (1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

##### (2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.

Therefore, avoid this type of connection.

##### (3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

### Latch-Up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

- (1) Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
- (2) Be sure that abnormal current flows do not occur during the power-on sequence.

### Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

### Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

### Precautions Related to Usage of Devices

Spanion semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

### 6.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Spanion's recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Spanion recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

### **Surface Mount Type**

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Spansion recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Spansion ranking of recommended conditions.

### **Lead-Free Packaging**

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

### **Storage of Semiconductor Devices**

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

- (1) Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product.  
Store products in locations where temperature changes are slight.
- (2) Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5 °C and 30 °C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
- (3) When necessary, Spansion packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
- (4) Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

### **Baking**

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Spansion recommended conditions for baking.

Condition: 125°C/24 h

### **Static Electricity**

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

- (1) Maintain relative humidity in the working environment between 40% and 70%.  
Use of an apparatus for ion generation may be needed to remove electricity.
- (2) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
- (3) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).  
Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
- (4) Ground all fixtures and instruments, or protect with anti-static measures.
- (5) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.



### 6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

(5) Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Spansion products in other special environmental conditions should consult with sales representatives.

Please check the latest handling precautions at the following URL.

<http://www.spansion.com/fjdocuments/fj/datasheet/e-ds/DS00-00004.pdf>

## 7. Handling Devices

### Power Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Moreover, connect the current supply source with each Power supply pin and GND pin of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1  $\mu\text{F}$  be connected as a bypass capacitor between each Power supply pin and GND pin, between AVCC pin and AVSS pin near this device.

### Stabilizing Supply Voltage

A malfunction may occur when the power supply voltage fluctuates rapidly even though the fluctuation is within the recommended operating conditions of the VCC power supply voltage. As a rule, with voltage stabilization, suppress the voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the VCC value in the recommended operating conditions, and the transient fluctuation rate does not exceed 0.1 V/ $\mu\text{s}$  when there is a momentary fluctuation on switching the power supply.

### Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator, and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane as this is expected to produce stable operation.

Evaluate oscillation of your using crystal oscillator by your mount board.

### Sub Crystal Oscillator

This series sub oscillator circuit is low gain to keep the low current consumption. The crystal oscillator to fill the following conditions is recommended for sub crystal oscillator to stabilize the oscillation.

#### ■ Surface mount type

Size: More than 3.2 mm  $\times$  1.5 mm

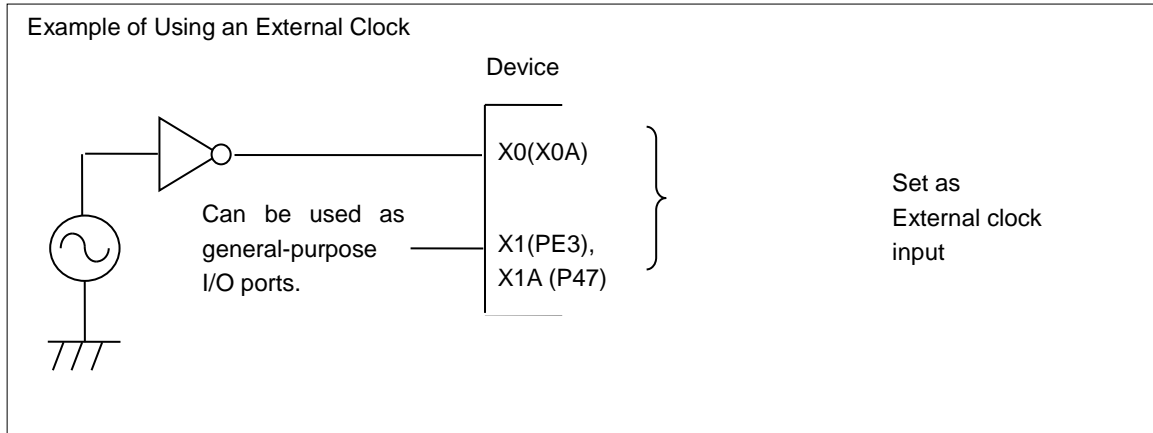
Load capacitance: Approximately 6 pF to 7 pF

#### ■ Lead type

Load capacitance: Approximately 6 pF to 7 pF

**Using an External Clock**

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input, and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

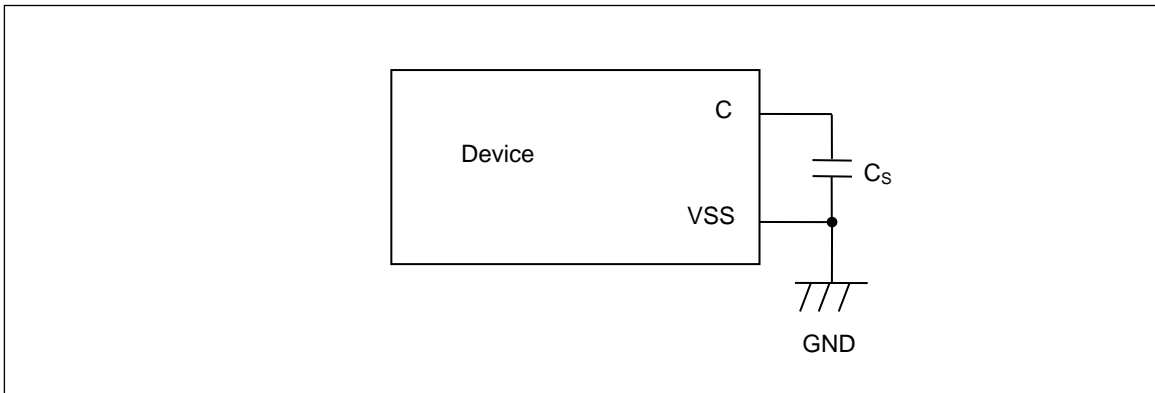


**Handling when Using Multi-Function Serial Pin as I<sup>2</sup>C Pin**

If it is using the multi-function serial pin as I<sup>2</sup>C pins, P-ch transistor of digital output is always disabled. However, I<sup>2</sup>C pins need to keep the electrical characteristic like other pins and not to connect to the external I<sup>2</sup>C bus system with power OFF.

**C Pin**

This series contains the regulator. Be sure to connect a smoothing capacitor (C<sub>s</sub>) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. However, some laminated ceramic capacitors have the characteristics of capacitance variation due to thermal fluctuation (F characteristics and Y5V characteristics). Please select the capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of a capacitor. A smoothing capacitor of about 4.7 μF would be recommended for this series.



**Mode Pins (MD0)**

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, as well as the distance between the mode pins and VCC pins or VSS pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

**Notes on Power-on**

Turn power on/off in the following order or at the same time.

Turning on : VBAT → VCC  
                  VCC → AVCC → AVRH  
Turning off : VCC → VBAT  
                  AVRH → AVCC → VCC

**Serial Communication**

There is a possibility to receive wrong data due to the noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider the case of receiving wrong data due to noise; perform error detection such as by applying a checksum of data at the end. If an error is detected, retransmit the data.

**Differences in Features Among the Products with Different Memory Sizes and Between Flash Memory Products and MASK Products**

The electric characteristics including power consumption, ESD, latch-up, noise characteristics, and oscillation characteristics among the products with different memory sizes and between Flash memory products and MASK products are different because chip layout and memory structures are different.

If you are switching to use a different product of the same series, please make sure to evaluate the electric characteristics.

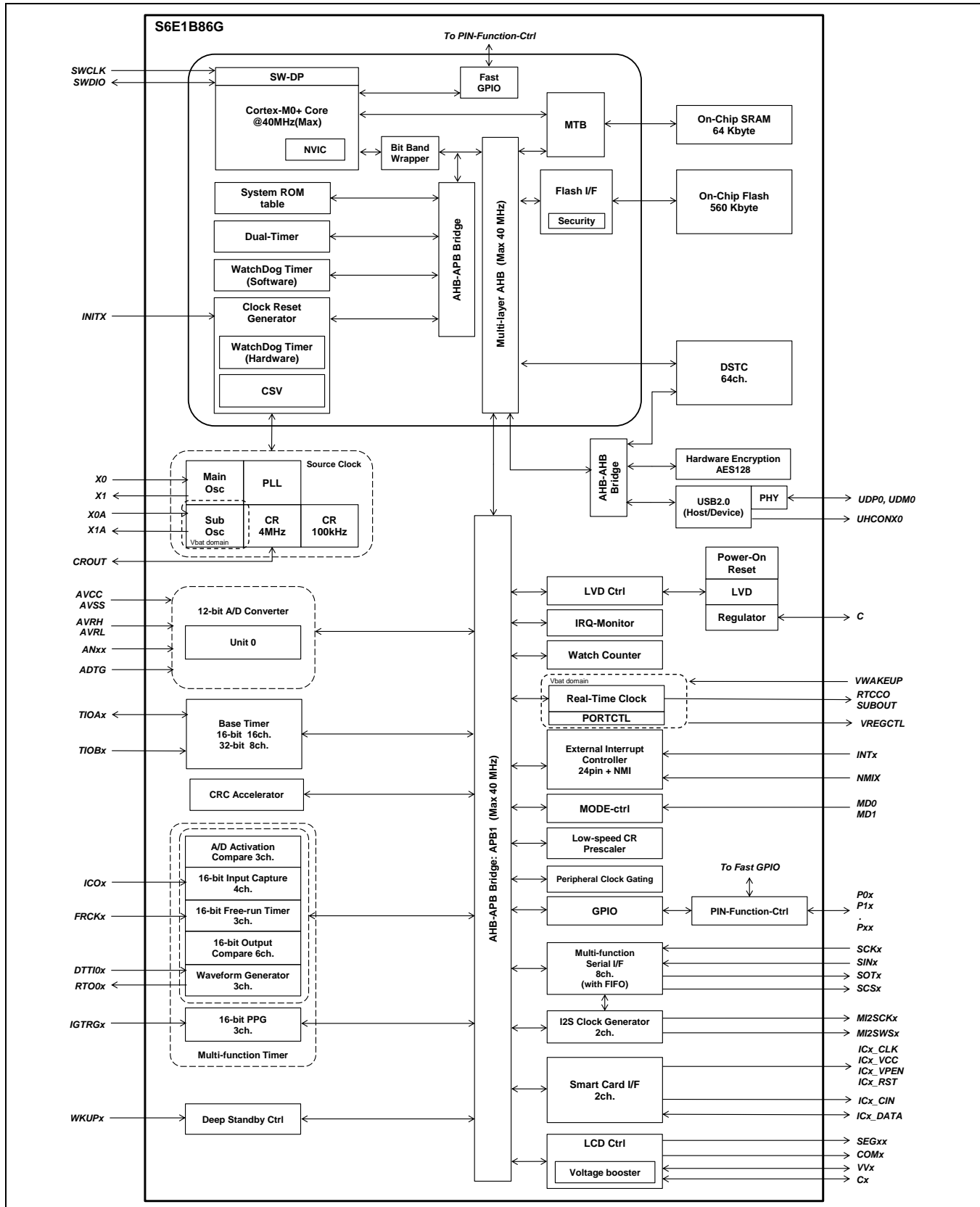
**Pull-Up Function of 5 V Tolerant I/O**

Please do not input the signal more than VCC voltage at the time of Pull-Up function use of 5 V tolerant I/O.

**Handling when Using Debug Pins**

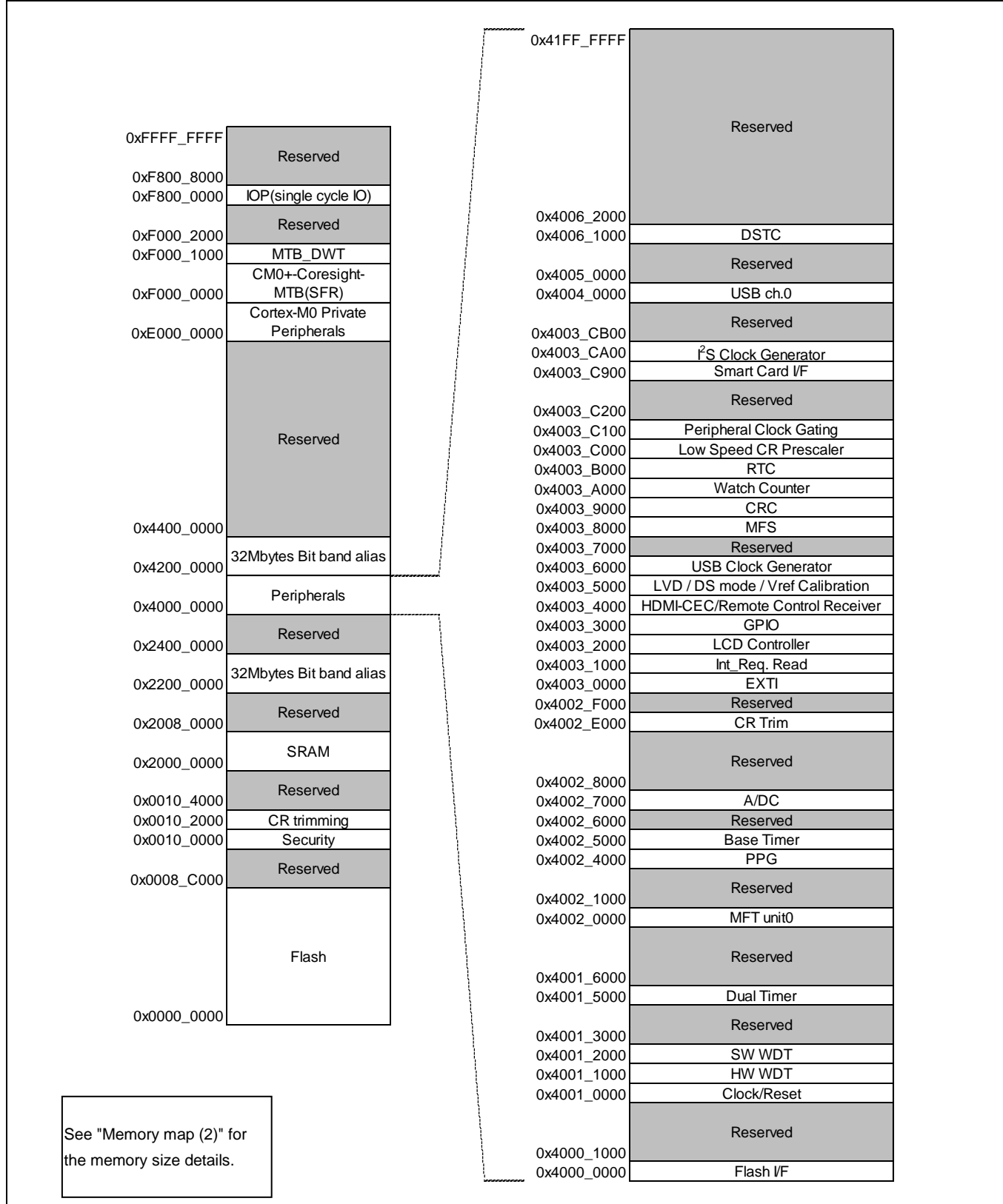
When debug pins (SWDIO/SWCLK) are set to GPIO or other peripheral functions, set them as output only; do not set them as input.

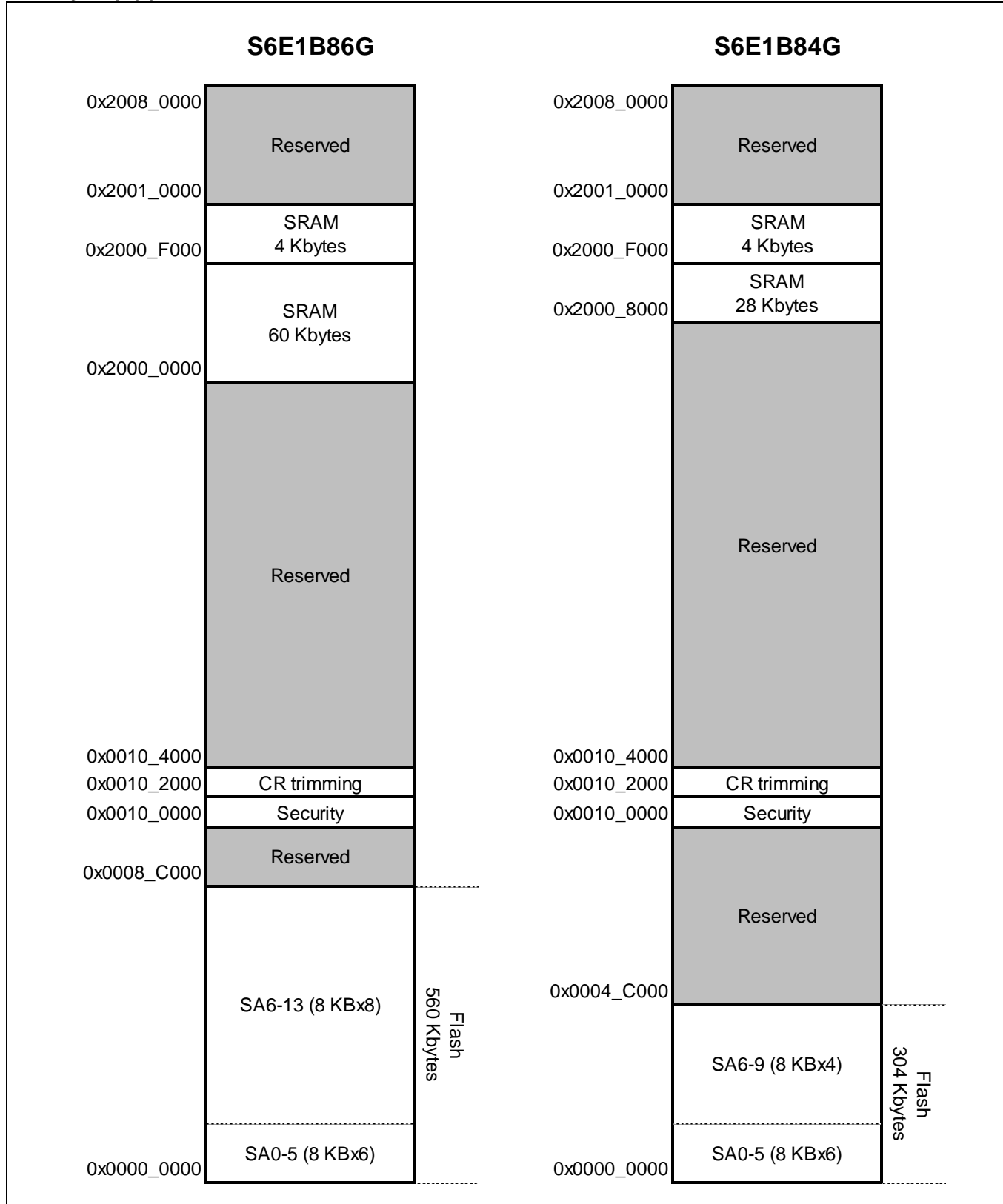
**8. Block Diagram**



## 9. Memory Map

### Memory Map (1)



**Memory Map (2)**


\*: See "S6E1B8 Series Flash Programming Manual" to check details of the Flash memory.

**Peripheral Address Map**

Start Address	End Address	Bus	Peripheral	
0x4000_0000	0x4000_0FFF	AHB	Flash memory I/F register	
0x4000_1000	0x4000_FFFF		Reserved	
0x4001_0000	0x4001_0FFF	APB0	Clock/Reset Control	
0x4001_1000	0x4001_1FFF		Hardware Watchdog Timer	
0x4001_2000	0x4001_2FFF		Software Watchdog Timer	
0x4001_3000	0x4001_4FFF		Reserved	
0x4001_5000	0x4001_5FFF		Dual-Timer	
0x4001_6000	0x4001_FFFF		Reserved	
0x4002_0000	0x4002_0FFF		APB1	Multi-function Timer unit0
0x4002_1000	0x4002_3FFF	Reserved		
0x4002_4000	0x4002_4FFF	PPG		
0x4002_5000	0x4002_5FFF	Base Timer		
0x4002_6000	0x4002_6FFF	Reserved		
0x4002_7000	0x4002_7FFF	A/D Converter		
0x4002_8000	0x4002_DFFF	Reserved		
0x4002_E000	0x4002_EFFF	Built-in CR trimming		
0x4002_F000	0x4002_FFFF	Reserved		
0x4003_0000	0x4003_0FFF	External Interrupt Controller		
0x4003_1000	0x4003_1FFF	Interrupt Request Batch-Read Function		
0x4003_2000	0x4003_2FFF	LCD Controller		
0x4003_3000	0x4003_3FFF	GPIO		
0x4003_4000	0x4003_4FFF	HDMI-CEC/ Remote Control Receiver		
0x4003_5000	0x4003_5FFF	Low-Voltage Detection / DS mode / Vref Calibration		
0x4003_6000	0x4003_6FFF	USB Clock Generator		
0x4003_7000	0x4003_7FFF	Reserved		
0x4003_8000	0x4003_8FFF	Multi-function Serial Interface		
0x4003_9000	0x4003_9FFF	CRC		
0x4003_A000	0x4003_AFFF	Watch Counter		
0x4003_B000	0x4003_BFFF	Real-time clock		
0x4003_C000	0x4003_C0FF	Low-speed CR Prescaler		
0x4003_C100	0x4003_C7FF	Peripheral Clock Gating		
0x4003_C800	0x4003_FFFF	Reserved		
0x4003_C900	0x4003_C9FF	Smart Card Interface		
0x4003_CA00	0x4003_CAFF	I <sup>2</sup> S Clock Generator		
0x4003_CB00	0x4003_FFFF	Reserved		
0x4004_0000	0x4005_FFFF	AHB		USB ch.0
0x4006_0000	0x4006_0FFF			Reserved
0x4006_1000	0x4006_1FFF			DSTC
0x4006_2000	0x41FF_FFFF			Reserved



## 10. Pin Status in Each CPU State

The terms used for pin status have the following meanings.

- INITX=0  
This is the period when the INITX pin is the "L" level.
- INITX=1  
This is the period when the INITX pin is the "H" level.
- SPL=0  
This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "0".
- SPL=1  
This is the status that the standby pin level setting bit (SPL) in the Standby Mode Control Register (STB\_CTL) is set to "1".
- Input enabled  
Indicates that the input function can be used.
- Internal input fixed at "0"  
This is the status that the input function cannot be used. Internal input is fixed at "L".
- Hi-Z  
Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.
- Setting disabled  
Indicates that the setting is disabled.
- Maintain previous state  
Maintains the state in which a pin was immediately prior to entering the current mode.  
If a built-in peripheral function is operating, the output follows the peripheral function.  
If the pin is being used as a port, that output is maintained.
- Analog input is enabled  
Indicates that the analog input is enabled.
- Trace output  
Indicates that the trace function can be used.
- GPIO selected  
In Deep standby mode, pins switch to the general-purpose I/O port.

**List of Pin Status**

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ External main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Main crystal oscillator output pin	Hi-Z / Internal input fixed at 0/ Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state/When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*1, Hi-Z / Internal input fixed at 0
C	INITX input pin	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled	Pull-up / Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
E	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Input enabled	Input enabled	Input enabled
	Sub crystal oscillator input pin / External sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
F	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	External sub clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state	Hi-Z / Internal input fixed at 0	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z / Internal input fixed at 0 / Input enabled	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Maintain previous state	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0	Maintain previous state / When oscillation stops*2, Hi-Z / Internal input fixed at 0
G	NMIX selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
H	Serial wire debug selected	Hi-Z	Pull-up / Input enabled	Pull-up / Input enabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
I	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	GPIO selected									
J	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected
	Resource other than the above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0			
	GPIO selected									
K	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	Resource other than the above selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	GPIO selected									

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
L	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0
	Resource other than the above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected						Hi-Z / Internal input fixed at 0			
M	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Input enabled	GPIO selected	Hi-Z / Input enabled	GPIO selected
N	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0		
	Resource other than above selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled			Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0		
	GPIO selected	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0						

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State	
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	
O	CEC enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0	
	External interrupt enabled selected							GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0		
	Resource other than above selected							Hi-Z	Hi-Z / Input enabled		Hi-Z / Input enabled
	GPIO selected										
P	Resource selected	Hi-Z	Hi-Z / Input enabled	Hi-Z / Input enabled	Maintain previous State	Maintain previous State	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected	
	GPIO selected										
Q	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected	
	USB IO					Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled	Hi-Z/Input enabled	
	GPIO selected	Hi-Z	Hi-Z/Input enabled	Hi-Z/Input enabled		Maintain previous state	Hi-Z	GPIO	Hi-Z	GPIO	

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
R	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Output maintains previous state / Internal input fixed at 0			
	GPIO selected									
S	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0			Output Maintain previous state / Internal input fixed at 0
	GPIO selected							Output Maintain previous state / Internal input fixed at 0		

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
T	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0		
	Resource other than above selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Output maintains previous state / Internal input fixed at 0	
	GPIO selected		Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Output maintains previous state / Internal input fixed at 0			



Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
U	CEC enabled				Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled			Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	GPIO selected / Internal input fixed at 0
	External interrupt enabled selected						Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0						
V	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	State Upon Power-on Reset or Low-Voltage Detection	State at INITX Input	State Upon Device Internal Reset	State in Run Mode or Sleep Mode	State in Timer Mode, RTC Mode, or Stop Mode		State in Deep Standby RTC Mode or Deep Standby Stop Mode State		State when Return from Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable	Power Supply Stable	Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Analog input selected	Hi-Z	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled	Hi-Z / Internal input fixed at 0 / Analog input enabled
	WKUP enabled						Hi-Z / Internal input fixed at 0	WKUP input enabled	Hi-Z / WKUP input enabled	
	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	GPIO selected / Internal input fixed at 0
	Resource other than above selected						Hi-Z / Internal input fixed at 0			
	GPIO selected									
X	External interrupt enabled selected	Setting disabled	Setting disabled	Setting disabled			Maintain previous state	GPIO selected / Internal input fixed at 0		
	Resource other than above selected				Maintain previous state	Maintain previous state	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0
	GPIO selected	Hi-Z	Hi-Z / Internal input fixed at 0	Hi-Z / Internal input fixed at 0			Hi-Z / Internal input fixed at 0	Output Maintain previous state / Internal input fixed at 0		

\*1: Oscillation stops in Sub timer mode, Low-speed CR timer mode, Stop mode, RTC mode.

\*2: Oscillation stops in Stop mode.

## 11. Electrical Characteristics

### 11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage* <sup>1</sup> , * <sup>2</sup>	$V_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 4.6$	V	
Analog power supply voltage* <sup>1</sup> , * <sup>3</sup>	$AV_{CC}$	$V_{SS} - 0.5$	$V_{SS} + 4.6$	V	
Analog reference voltage* <sup>1</sup> , * <sup>3</sup>	$AVRH$	$V_{SS} - 0.5$	$V_{SS} + 4.6$	V	
Input voltage* <sup>1</sup>	$V_I$	$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 4.6$ V)	V	
		$V_{SS} - 0.5$	$V_{SS} + 6.5$	V	5 V tolerant
Analog pin input voltage* <sup>1</sup>	$V_{IA}$	$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 4.6$ V)	V	
Output voltage* <sup>1</sup>	$V_O$	$V_{SS} - 0.5$	$V_{CC} + 0.5$ ( $\leq 4.6$ V)	V	
L level maximum output current* <sup>4</sup>	$I_{OL}$	-	10	mA	
			39	mA	P0B / P0C
L level average output current* <sup>5</sup>	$I_{OLAV}$	-	4	mA	
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total average output current* <sup>6</sup>	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current* <sup>4</sup>	$I_{OH}$	-	- 10	mA	
			- 39	mA	P0B / P0C
H level average output current* <sup>5</sup>	$I_{OHAV}$	-	- 4	mA	
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current* <sup>6</sup>	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	$P_D$	-	250	mW	
Storage temperature	$T_{STG}$	- 55	+ 150	°C	

\*1: These parameters are based on the condition that  $V_{SS}=AV_{SS}=0$  V.

\*2:  $V_{CC}$  must not drop below  $V_{SS} - 0.5$  V.

\*3: Ensure that the voltage does not to exceed  $V_{CC} + 0.5$  V at power-on.

\*4: The maximum output current is the peak value for a single pin.

\*5: The average output is the average current for a single pin over a period of 100 ms.

\*6: The total average output current is the average current for all pins over a period of 100 ms.

\*7: When P0C/UDP0 and P0B/UDM0 pins are used as GPIO (P0C, P0B).

\*8: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

#### <WARNING>

- Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

**11.2 Recommended Operating Conditions**

(V<sub>SS</sub>=AV<sub>SS</sub>=0.0 V)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply voltage	V <sub>CC</sub>	-	1.65 *5	3.6	V	*1
			2.2	3.6	V	*2
			3.0	3.6	V	*3
LCD input voltage	V <sub>VV4</sub>	-	2.2	V <sub>CC</sub>	V	No booster used
		-	2.2	4.7	V	Booster is used
LCD External Capacitor *6	C <sub>f</sub> , C <sub>VV1</sub> , C <sub>VV2</sub> , C <sub>VV3</sub> , C <sub>VV4</sub>	-	0.5	1.3	μF	Booster is used
Sub Oscillation frequency *7	Fin	-	-	-	kHz	Typical is 32.768 kHz
Analog power supply voltage	AV <sub>CC</sub>	-	1.65	3.6	V	AV <sub>CC</sub> =V <sub>CC</sub>
Analog reference voltage	AVRH	-	2.7	AV <sub>CC</sub>	V	AV <sub>CC</sub> ≥ 2.7 V
			AV <sub>CC</sub>	AV <sub>CC</sub>	V	AV <sub>CC</sub> < 2.7 V
Smoothing capacitor	C <sub>S</sub>	-	1	10	μF	For regulator*4
Operating temperature	T <sub>A</sub>	-	- 40	+ 105	°C	

\*1: When LCD Controller is not used.

\*2: When LCD Controller is used.

\*3: When P0C/UDP0 and P0B/UDM0 pins are used as USB (UDP0, UDM0).

\*4: See "C Pin" in "7. Handling Devices" for the connection of the smoothing capacitor.

\*5: In between less than the minimum power supply voltage reset / interrupt detection voltage or more, instruction execution and low voltage detection function by built-in High-speed CR (including Main PLL is used) or built-in Low-speed CR is possible to operate only.

\*6: LCD external capacitor between VVx to VSS, and between C0 and C1.

\*7: If a Booster is used, Sub OSC should provide operation clock at typically 32.768 kHz.

**<WARNING>**

1. The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
2. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
3. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.
4. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

**11.3 DC Characteristics**

**11.3.1 Current Rating**

Symbol (Pin Name)	Conditions	HCLK Frequency <sup>4</sup>	Value		Unit	Remarks		
			Typ <sup>1</sup>	Max <sup>2</sup>				
I <sub>CC</sub> (VCC)	Run mode, code executed from Flash	4 MHz external clock input, PLL ON <sup>8</sup> NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.7	TBD	mA	*3	
			8 MHz	1.15	TBD			
			20 MHz	2.25	TBD			
			40 MHz	4.5	TBD			
			4 MHz external clock input, PLL ON <sup>8</sup> Benchmark code executed Built-in high speed CR stopped PCLK1 stopped	4 MHz	0.75	TBD	mA	*3
			8 MHz	1.25	TBD			
			20 MHz	2.5	TBD			
			40 MHz	5.0	TBD			
			4 MHz crystal oscillation, PLL ON <sup>8</sup> NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.8	TBD	mA	*3
			8 MHz	1.4	TBD			
			20 MHz	2.75	TBD			
			40 MHz	5.5	TBD			
		Run mode, code executed from RAM	4 MHz external clock input, PLL ON <sup>8</sup> NOP code executed Built-in high speed CR stopped All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3
			8 MHz	1.2	TBD			
			20 MHz	2.4	TBD			
			40 MHz	4.8	TBD			
	Run mode, code executed from Flash	4 MHz external clock input, PLL ON NOP code executed Built-in high speed CR stopped PCLK1 stopped	40 MHz	2.6	TBD	mA	*3,*6,*7	
	Run mode, code executed from Flash	Built-in high speed CR <sup>5</sup> NOP code executed All peripheral clock stopped by CKENx	4 MHz	1.2	TBD			
		32 kHz crystal oscillation NOP code executed All peripheral clock stopped by CKENx	32 kHz	96	TBD			
		Built-in low speed CR NOP code executed All peripheral clock stopped by CKENx	100 kHz	120	TBD			
I <sub>CCS</sub> (VCC)	Sleep operation	4 MHz external clock input, PLL ON <sup>8</sup> All peripheral clock stopped by CKENx	4 MHz	0.6	TBD	mA	*3	
			8 MHz	1.1	TBD			
			20 MHz	1.9	TBD			
			40 MHz	3.2	TBD			
			Built-in high speed CR <sup>5</sup> All peripheral clock stopped by CKENx	4 MHz	0.5	TBD	mA	*3
			32 kHz crystal oscillation All peripheral clock stopped by CKENx	32 kHz	94	TBD		
			Built-in low speed CR All peripheral clock stopped by CKENx	100 kHz	105	TBD		

\*1 : T<sub>A</sub>=+25°C, V<sub>CC</sub>=3.3 V

\*2 : T<sub>A</sub>=+105°C, V<sub>CC</sub>=3.6 V

\*3 : All ports are fixed

\*4 : PCLK0 is set to divided rate 8

\*5 : The frequency is set to 4 MHz by trimming

\*6 : Flash sync down is set to FRWTR.RWT=11 and FSYNDN.SD=1111

\*7 : VCC=1.65 V

\*8 : When HCLK=4 MHz, PLL OFF

Parameter	Symbol (Pin Name)	Conditions	Value		Unit	Remarks	
			Typ	Max			
Power supply current	I <sub>CCH</sub> (VCC)	Stop mode	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V	10	TBD	μA	*1
			T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	9	TBD	μA	*1
			T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V	-	TBD	μA	*1
	I <sub>CCT</sub> (VCC)	Sub timer mode	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V 32 kHz Crystal oscillation	13	TBD	μA	*1
			T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V 32 kHz Crystal oscillation	12	TBD	μA	*1
			T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V 32 kHz Crystal oscillation	-	TBD	μA	*1
	I <sub>CCR</sub> (VCC)	RTC mode	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V 32 kHz Crystal oscillation	10.5	TBD	μA	*1
			T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V 32 kHz Crystal oscillation	9.5	TBD	μA	*1
			T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V 32 kHz Crystal oscillation	-	TBD	μA	*1

\*1: All ports are fixed. LVD off. Flash off.

Parameter	Symbol (Pin Name)	Conditions			Value		Unit	Remarks
					Typ	Max		
Power supply current	I <sub>CCHD</sub> (VCC)	Deep standby Stop mode	RAM off	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V	0.75	TBD	μA	*1
				T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	0.7	TBD	μA	*1
				T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V	-	TBD	μA	*1
			RAM on	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V	1.1	TBD	μA	*1
				T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	1.0	TBD	μA	*1
				T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V	-	TBD	μA	*1
	I <sub>CCRD</sub> (VCC)	Deep standby RTC mode	RAM off	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V	1.7	TBD	μA	*1
				T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	1.6	TBD	μA	*1
				T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V	-	TBD	μA	*1
			RAM on	T <sub>A</sub> =25°C V <sub>CC</sub> =3.3 V	1.9	TBD	μA	*1
				T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	1.7	TBD	μA	*1
				T <sub>A</sub> =105°C V <sub>CC</sub> =3.6 V	-	TBD	μA	*1

\*1: All ports are fixed. LVD off.

Parameter	Symbol (Pin Name)	Conditions	Value		Unit	Remarks	
			Typ	Max			
Power supply current	I <sub>CCVBAT</sub> (VBAT)	T <sub>A</sub> =25°C V <sub>CC</sub> =3.0V 32 kHz Crystal oscillation	0.9	TBD	μA	*1	
		T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V 32 kHz Crystal oscillation	0.8	TBD	μA	*1	
		T <sub>A</sub> =105°C V <sub>CC</sub> =3.6V 32 kHz Crystal oscillation	-	TBD	μA	*1	
		RTC stop	T <sub>A</sub> =25°C V <sub>CC</sub> =3.0V	0.05	TBD	μA	*1
			T <sub>A</sub> =25°C V <sub>CC</sub> =1.65 V	0.02	TBD	μA	*1
			T <sub>A</sub> =105°C V <sub>CC</sub> =3.6V	-	TBD	μA	*1

\*1: All ports are fixed.



**LVD Current**

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Low-Voltage detection circuit (LVD) power supply current	I <sub>CC</sub> LVD	VCC	At operation	0.13	TBD	μA	For occurrence of reset
				0.13	TBD	μA	For occurrence of interrupt

**Flash Memory Current**

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Flash memory write/erase current	I <sub>CC</sub> FLASH	VCC	At Write/Erase	9.5	TBD	mA	

**A/D converter Current**

(V<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Typ	Max		
Power supply current	I <sub>CC</sub> AD	AVCC	At operation	0.7	TBD	mA	
			At stop	0.13	TBD	μA	
Reference power supply current (AVRH)	I <sub>CC</sub> AVRH	AVRH	At operation	1.1	TBD	mA	AVRH=3.6 V
			At stop	0.1	TBD	μA	

**Peripheral Current Dissipation**

(V<sub>CC</sub>= 3.3 V, T<sub>A</sub>=25°C)

Clock System	Peripheral	Conditions	Frequency (MHz)				Unit	Remarks
			4	8	20	40		
HCLK	GPIO	At all ports operation	0.02	0.04	0.11	0.22	mA	
	DSTC	At 2ch operation	0.07	0.15	0.37	0.74		
PCLK1	Base timer	At 4ch operation	0.02	0.04	0.08	0.16	mA	
	Multi-functional timer/PPG	At 1 unit/4ch operation	0.06	0.11	0.28	0.55		
	ADC	At 1 unit operation	0.02	0.04	0.10	0.20		
	Multi-function serial	At 1ch operation	0.03	0.06	0.16	0.31		

**11.3.2 Pin Characteristics**

(V<sub>CC</sub>=AV<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V <sub>IHS</sub>	CMOS hysteresis input pin, MD0, MD1	V <sub>CC</sub> ≥ 2.7 V	V <sub>CC</sub> × 0.8	-	V <sub>CC</sub> +0.3	V	
			V <sub>CC</sub> < 2.7 V	V <sub>CC</sub> × 0.7				
		5 V tolerant input pin	V <sub>CC</sub> ≥ 2.7 V	V <sub>CC</sub> × 0.8	-	V <sub>SS</sub> +5.5		
			V <sub>CC</sub> < 2.7 V	V <sub>CC</sub> × 0.7				
L level input voltage (hysteresis input)	V <sub>ILS</sub>	CMOS hysteresis input pin, MD0, MD1	V <sub>CC</sub> ≥ 2.7 V	V <sub>SS</sub> - 0.3	-	V <sub>CC</sub> × 0.2	V	
			V <sub>CC</sub> < 2.7 V			V <sub>CC</sub> × 0.3		
		5 V tolerant input pin	V <sub>CC</sub> ≥ 2.7 V	V <sub>SS</sub> - 0.3	-	V <sub>CC</sub> × 0.2		
			V <sub>CC</sub> < 2.7 V			V <sub>CC</sub> × 0.3		
H level output voltage	V <sub>OH</sub>	4 mA type	V <sub>CC</sub> ≥ 2.7 V, I <sub>OH</sub> = - 4 mA	V <sub>CC</sub> - 0.5	-	V <sub>CC</sub>	V	
			V <sub>CC</sub> < 2.7 V, I <sub>OH</sub> = - 2 mA	V <sub>CC</sub> - 0.45				
		The pin doubled as USB I/O	-	USBV <sub>CC</sub> - 0.4	-	USBV <sub>CC</sub>	V	
L level output voltage	V <sub>OL</sub>	4 mA type	V <sub>CC</sub> ≥ 2.7 V, I <sub>OL</sub> = 4 mA	V <sub>SS</sub>	-	0.4	V	
			V <sub>CC</sub> < 2.7 V, I <sub>OL</sub> = 2 mA					
		The pin doubled as USB I/O	-	V <sub>SS</sub>	-	0.4	V	
Input leak current	I <sub>IL</sub>	-	-	- 5	-	+ 5	µA	
Pull-up resistance value	R <sub>PU</sub>	Pull-up pin	V <sub>CC</sub> ≥ 2.7 V	21	33	66	kΩ	
			V <sub>CC</sub> < 2.7 V	-	-	134		
Input capacitance	C <sub>IN</sub>	Other than V <sub>CC</sub> , USBV <sub>CC</sub> , V <sub>SS</sub> , AV <sub>CC</sub> , AV <sub>SS</sub> , AVRH	-	-	5	15	pF	

**11.3.3 LCD Characteristic**

11.3.3.1 LCD Characteristic Without Booster

( $V_{CC} = AV_{CC} = 1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to }+105^\circ\text{C}$ )

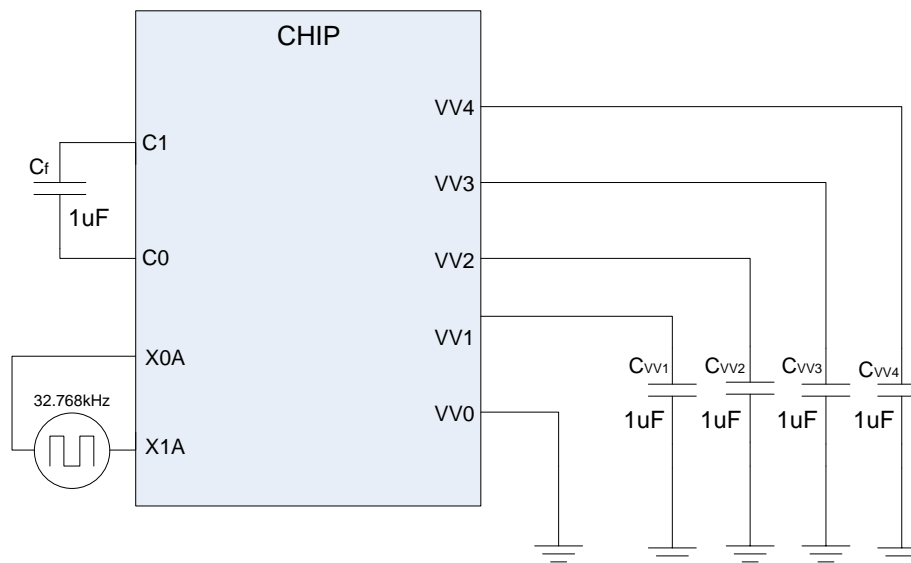
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
VV0 to VV3 output voltage (1/4 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	$V_{V4} \times 5\%$	V	
	V <sub>V1</sub>	VV1		$V_{V4} \times 1/4$ -10%	-	$V_{V4} \times 1/4$ +10%		
	V <sub>V2</sub>	VV2		$V_{V4} \times 1/2$ -10%	-	$V_{V4} \times 1/2$ +10%		
	V <sub>V3</sub>	VV3		$V_{V4} \times 3/4$ -10%	-	$V_{V4} \times 3/4$ +10%		
VV0 to VV3 output voltage (1/3 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	$V_{V4} \times 5\%$	V	
	V <sub>V1</sub>	VV1		$V_{V4} \times 1/3$ -10%	-	$V_{V4} \times 1/3$ +10%		
	V <sub>V2</sub>	VV2		$V_{V4} \times 2/3$ -10%	-	$V_{V4} \times 2/3$ +10%		
	V <sub>V3</sub>	VV3		$V_{V4} \times 2/3$ -10%	-	$V_{V4} \times 2/3$ +10%		
VV0 to VV3 output voltage (1/2 bias)	V <sub>V0</sub>	VV0	When using internal dividing register	0	-	$V_{V4} \times 5\%$	V	
	V <sub>V1</sub>	VV1		$V_{V4} \times 1/2$ -10%	-	$V_{V4} \times 1/2$ +10%		
	V <sub>V2</sub>	VV2		$V_{V4} \times 1/2$ -10%	-	$V_{V4} \times 1/2$ +10%		
	V <sub>V3</sub>	VV3		$V_{V4} \times 1/2$ -10%	-	$V_{V4} \times 1/2$ +10%		
VV4 Active current (1/4 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing resistor	-	10	TBD	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing resistor	-	100	TBD	μA	
VV4 Active current (1/3 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing resistor	-	12	TBD	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing resistor	-	120	TBD	μA	
VV4 Active current (1/2 bias)	I <sub>R100K</sub>	VV4	When using 100 kΩ internal dividing resistor	-	18	TBD	μA	
	I <sub>R10K</sub>	VV4	When using 10 kΩ internal dividing resistor	-	180	TBD	μA	
VV4 static current	I <sub>OFF_VV4</sub>	VV4	When LCD stops	-	0.5	TBD	μA	
VV0 output voltage in using external resistor	V <sub>V0E</sub>	VV0	I <sub>OL</sub> =1 mA	-	-	0.66	V	

11.3.3.2 LCD Characteristic With Booster

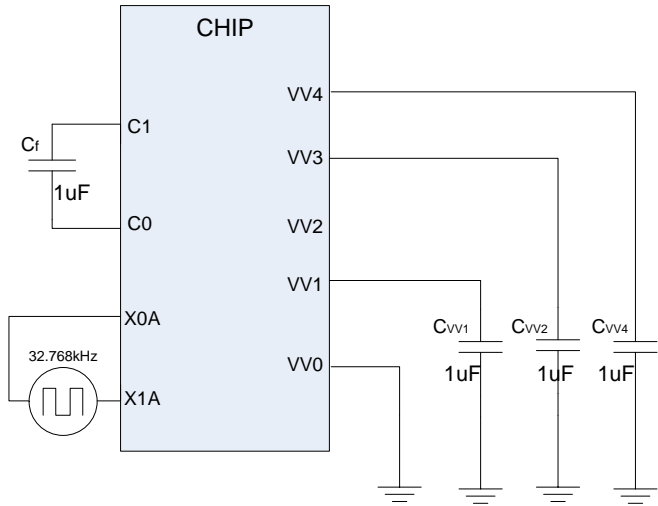
Recommended LCD Operation Conditions With Booster

( $V_{CC} = AV_{CC} = 1.65\text{ V to } 3.6\text{ V}$ ,  $V_{SS} = AV_{SS} = 0\text{ V}$ ,  $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ )

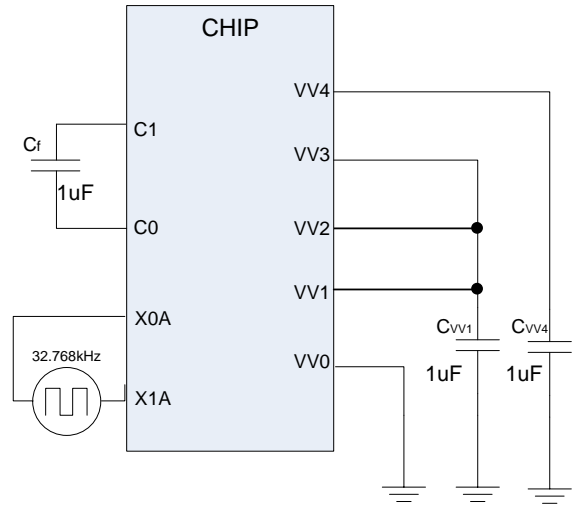
Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Voltage correlation	VCC-VV1	VCC, VV1	0.35	-	-	V	VCC-VV1 must be larger than 0.35 V
External input tolerant voltage	$V_{tole}$	VV1, VV2, VV3, VV4, C0, C1	0	-	5.5	V	
Operating frequency	$f_{IN}$	-	-	32.768	-	kHz	Crystal oscillator
External Capacitor	$C_f, C_{VV1}, C_{VV2}, C_{VV3}, C_{VV4}$	VV1, VV2, VV3, VV4, C0, C1	0.5	1	1.3	$\mu\text{F}$	
LCD capacitor	$C_{LCD/1COM}$	-	-	1.25	8	$\mu\text{F}$	
Frame period	$t_{FRAME}$	-	1/150	-	1/30	s	



LCD Booster 1/4 mode (BIAS[1:0]=2'b10)



LCD Booster 1/3 mode (BIAS[1:0]=2'b01)



LCD Booster 1/2 mode (BIAS[1:0]=2'b00)

DC Electrical Specifications of Internal reference output voltage setting

( $V_{CC} = AV_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$ ,  $V_{SS} = AV_{SS} = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks
			TRC[1:0]	TRF[3:0]	Min	Typ	Max		
Internal reference output voltage setting	VV1A	VV1	00	1010	0.89	1.00	1.11	V	BIAS[1:0]=10 <sup>*4</sup> Other BIAS[1:0]setting is inhibited
			00	1011	0.94	1.05	1.16		
			00	1100	0.99	1.10	1.21		
			00	1101	1.03	1.15	1.27		
			00	1110	1.07	1.20	1.38		
			01	0111	1.11	1.25	1.38	V	BIAS[1:0]=01 <sup>*3</sup> Other BIAS[1:0]setting is inhibited
			01	1000	1.16	1.30	1.44		
			01	1001	1.20	1.35	1.49		
			01	1010	1.25	1.40	1.55		
			01	1011	1.30	1.45	1.60		
			01	1100	1.34	1.50	1.65	V	BIAS[1:0]=00 <sup>*2</sup> Other BIAS[1:0]setting is inhibited
			01	1101	1.39	1.55	1.71		
			01	1110	1.44	1.60	1.76		
			10	0101	1.46	1.65	1.83		
			10	1100	1.79	2.00	2.21		
			10	1101	1.84	2.05	2.26	V	
			10	1110	1.89	2.10	2.32		
			11	0010	1.85	2.15	2.39		
11	0011	1.90	2.20	2.44					

Parameter	Symbol	Pin Name	Conditions		Value			Unit	Remarks	
			TRC[1:0]	TRF[3:0]	Min	Typ	Max			
Internal reference output voltage setting	VV1A	VV1	11	0100	1.96	2.25	2.49	V	BIAS[1:0]=00 *1 Other BIAS[1:0]setting is inhibited	
			11	0101	2.01	2.30	2.55			
			11	0110	2.06	2.35	2.60			
			11	0111	2.11	2.40	2.65			
			11	1000	2.17	2.45	2.75			
Charge Pump output voltage	V2	VV2	VV1=1.15 V BIAS1=1 BIAS0=0 *4			2.2	2.3	2.4	V	VV1=1.15[V]
	V3	VV3				3.3	3.45	3.6	V	
	V4	VV4				4.4	4.6	4.8	V	
	V2	VV2	VV1=1.5 V BIAS1=0 BIAS0=1 *3			2.9	3.0	3.1	V	VV1<(VCC-0.35)[V]
	V3	VV3				=VV2			V	
	V4	VV4				4.3	4.5	4.7	V	
	V2	VV2	VV1=2.25 V BIAS1=0 BIAS0=0 *2			=VV1			V	VV1<(VCC-0.35)[V]
	V3	VV3				=VV1			V	
	V4	VV4				4.3	4.5	4.7	V	

- \*1: Other setting combinations are inhibited
- \*2: Charge pump 1/2 mode
- \*3: Charge pump 1/3 mode
- \*4: Charge pump 1/4 mode

Transient Electrical Specifications

(V<sub>CC</sub> =AV<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Startup time	t <sub>ST</sub>	VV4	-	-	500	mS	When BSTPD change from 1 to 0

**11.4 AC Characteristics**

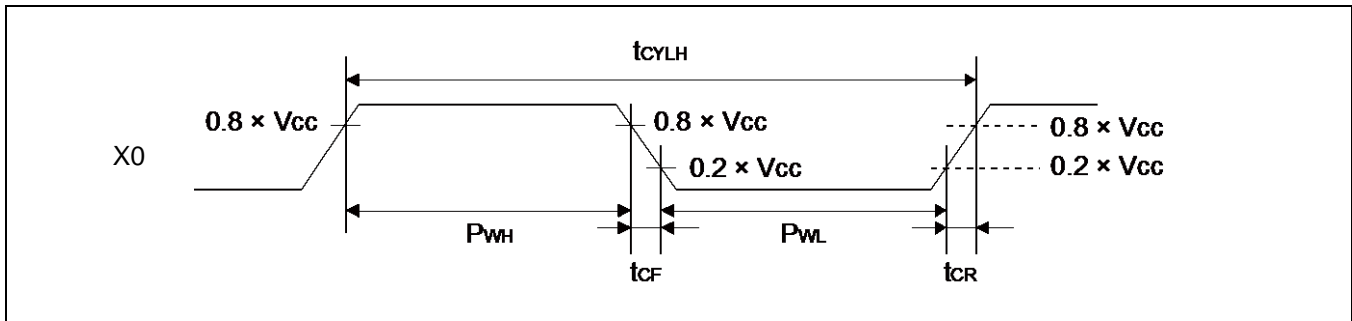
**11.4.1 Main Clock Input Characteristics**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	$f_{CH}$	X0, X1	$V_{CC} \geq 2.7\text{ V}$	4	48	MHz	When the crystal oscillator is connected
			$V_{CC} < 2.7\text{ V}$	4	20		
-	4		48	MHz	When the external clock is used		
Input clock cycle	$t_{CYLH}$		-			20.83	250
Input clock pulse width	-	$P_{WH}/t_{CYLH}$ , $P_{WL}/t_{CYLH}$	45	55	%	When the external clock is used	
Input clock rising time and falling time	$t_{CF}$ , $t_{CR}$	-	-	-	5	ns	When the external clock is used
Internal operating clock <sup>*1</sup> frequency	$f_{CM}$	-	-	-	40.8	MHz	Master clock
	$f_{CC}$	-	-	-	40.8	MHz	Base clock (HCLK/FCLK)
	$f_{CP0}$	-	-	-	40.8	MHz	APB0 bus clock <sup>*2</sup>
	$f_{CP1}$	-	-	-	40.8	MHz	APB1 bus clock <sup>*2</sup>
Internal operating clock <sup>*1</sup> cycle time	$t_{CYCC}$	-	-	24.5	-	ns	Base clock (HCLK/FCLK)
	$t_{CYCP0}$	-	-	24.5	-	ns	APB0 bus clock <sup>*2</sup>
	$t_{CYCP1}$	-	-	24.5	-	ns	APB1 bus clock <sup>*2</sup>

\*1: For details of each internal operating clock, refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

\*2: For details of the APB bus to which a peripheral is connected, see "8. Block Diagram".

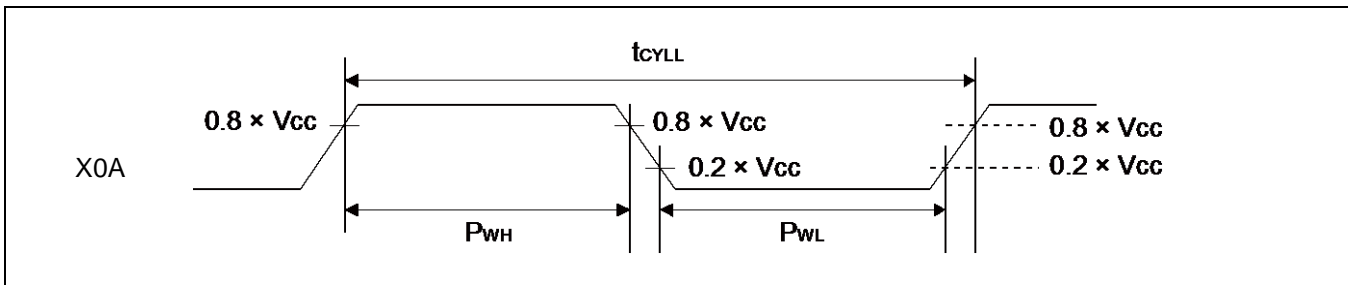


**11.4.2 Sub Clock Input Characteristics**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$f_{CL}$	X0A, X1A	-	-	32.768	-	kHz	When the crystal oscillator is connected*
			-	32	-	100	kHz	When the external clock is used
Input clock cycle	$t_{CYLL}$		-	10	-	31.25	$\mu\text{s}$	When the external clock is used
Input clock pulse width	-		$P_{WH}/t_{CYLL}$ , $P_{WL}/t_{CYLL}$	45	-	55	%	When the external clock is used

\*: See "Sub crystal oscillator" in "7. Handling Devices" for the crystal oscillator used.





**11.4.3 Built-in CR Oscillation Characteristics**

**Built-in High-Speed CR**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRH}$	$T_A = -20^\circ\text{C to }+85^\circ\text{C}$	3.96	4	4.04	MHz	During trimming <sup>*1</sup>
		$T_A = -40^\circ\text{C to }+105^\circ\text{C}$	3.92	4	4.08		
		$T_A = -40^\circ\text{C to }+105^\circ\text{C}$	2.6	4	5.2		Not during trimming
Frequency stabilization time	$t_{CRWT}$	-	-	-	30	$\mu\text{s}$	<sup>*2</sup>
					300	$\mu\text{s}$	If TRT is changed. <sup>*2</sup>

\*1: In the case of using the values in CR trimming area of Flash memory at shipment for frequency trimming/temperature trimming.

\*2: This is time from the trim value setting to stable of the frequency of the High-speed CR clock. After setting the trim value, the period when the frequency stability time passes can use the High-speed CR clock as a source clock.

**Built-in Low-Speed CR**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	$f_{CRL}$	-	50	100	150	kHz	

**11.4.4 Operating Conditions of Main PLL**

*(In the Case of Using the Main Clock as the Input Clock of the PLL)*

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (LOCK UP time)	$t_{LOCK}$	100	-	-	$\mu\text{s}$	
PLL input clock frequency	$f_{PLLI}$	4	-	16	MHz	
PLL multiple rate	-	5	-	37	multiple	
PLL macro oscillation clock frequency	$f_{PLLO}$	75	-	150	MHz	
Main PLL clock frequency* <sup>2</sup>	$f_{CLKPLL}$	-	-	40.8	MHz	
USB clock frequency* <sup>3</sup>	$f_{CLKSPLL}$	-	-	48	MHz	

\*1: The wait time is the time it takes for PLL oscillation to stabilize.

\*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

\*3: For more information about USB clock, see "Chapter: USB Clock Generation" in "FM0+ Family Peripheral Manual Communication Macro Part".

**11.4.5 Operating Conditions of Main PLL**

*(In the Case of Using the Built-in High-Speed CR Clock as the Input Clock of the Main PLL)*

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

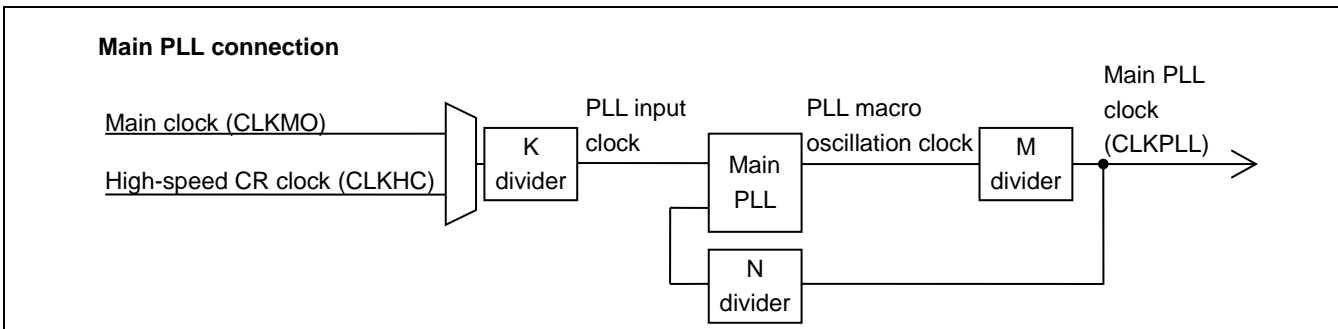
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time* <sup>1</sup> (LOCK UP time)	$t_{LOCK}$	100	-	-	$\mu\text{s}$	
PLL input clock frequency	$f_{PLLI}$	3.8	4	4.2	MHz	
PLL multiple rate	-	19	-	35	multiple	
PLL macro oscillation clock frequency	$f_{PLLO}$	72	-	150	MHz	
Main PLL clock frequency* <sup>2</sup>	$f_{CLKPLL}$	-	-	40.8	MHz	

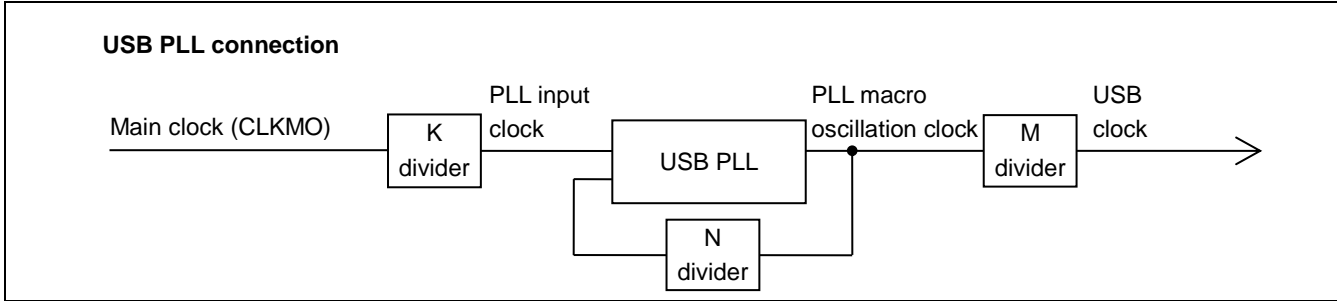
\*1: The wait time is the time it takes for PLL oscillation to stabilize.

\*2: For details of the main PLL clock (CLKPLL), refer to "Chapter: Clock" in "FM0+ Family Peripheral Manual".

**Note:**

- For the main PLL source clock, input the high-speed CR clock (CLKHC) whose frequency has been trimmed. When setting PLL multiple rate, please take the accuracy of the built-in High-speed CR clock into account and prevent the master clock from exceeding the maximum frequency.

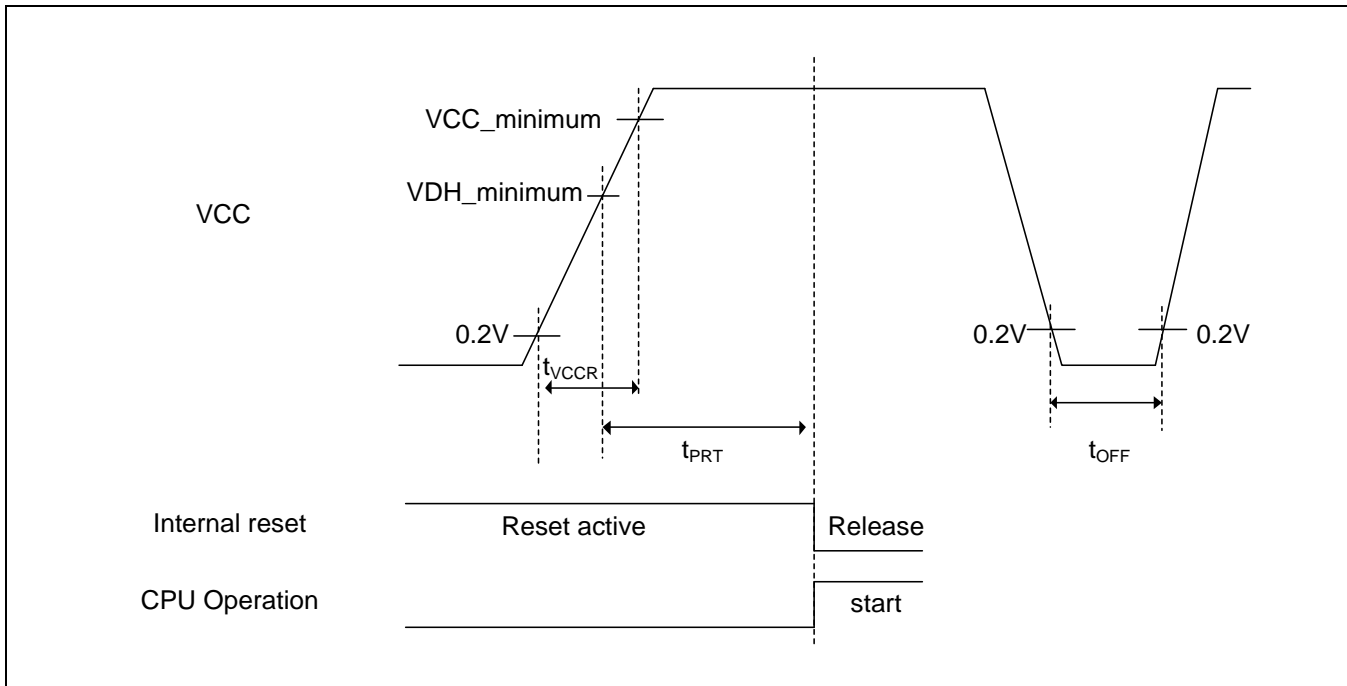



**11.4.6 Reset Input Characteristics**
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^\circ\text{C to }+105^\circ\text{C})$ 

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	$t_{INITX}$	INITX	-	500	-	ns	

**11.4.7 Power-on Reset Timing**
 $(V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}, V_{SS}=AV_{SS}=0\text{ V}, T_A=-40^\circ\text{C to }+105^\circ\text{C})$ 

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Power supply rising time	$t_{VCCR}$	VCC	0	-	ms	
Power supply shut down time	$t_{OFF}$		1	-	ms	
Time until releasing Power-on reset	$t_{PRT}$		0.43	3.4	ms	


**Glossary**

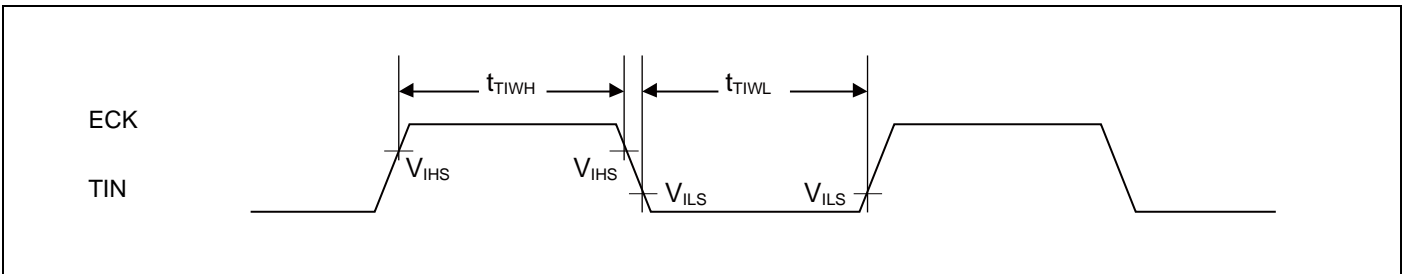
- VCC\_minimum : Minimum  $V_{CC}$  of recommended operating conditions.
- VDH\_minimum : Minimum detection voltage of Low-Voltage detection reset.

See "11.7 Low-Voltage Detection Characteristics".

**11.4.8 Base Timer Input Timing**
**Timer Input Timing**

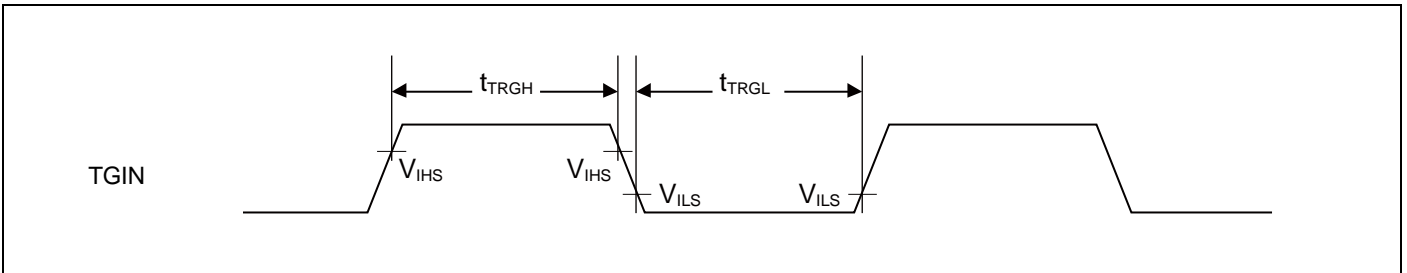
 ( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TIWH}$ , $t_{TIWL}$	TIOAn/TIOBn (when using as ECK, TIN)	-	$2 t_{CYCP}$	-	ns	


**Trigger Input Timing**

 ( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	$t_{TRGH}$ , $t_{TRGL}$	TIOAn/TIOBn (when using as TGIN)	-	$2 t_{CYCP}$	-	ns	


**Note:**

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
For the number of the APB bus to which the Base Timer has been connected, see "8. Block Diagram".

**11.4.9 CSIO/SPI/UART Timing**

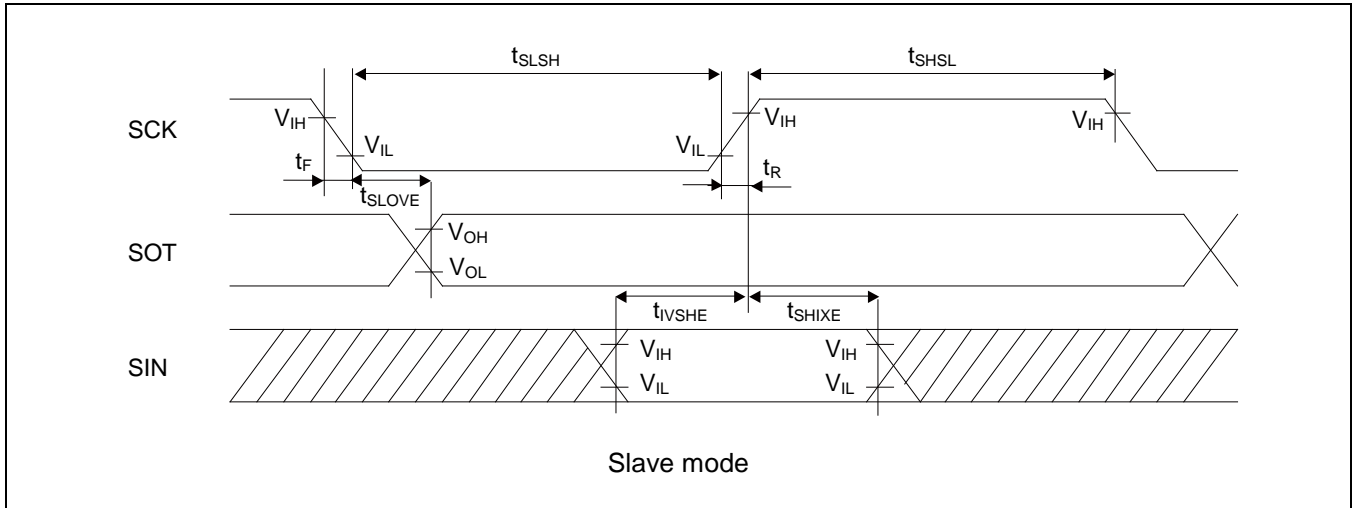
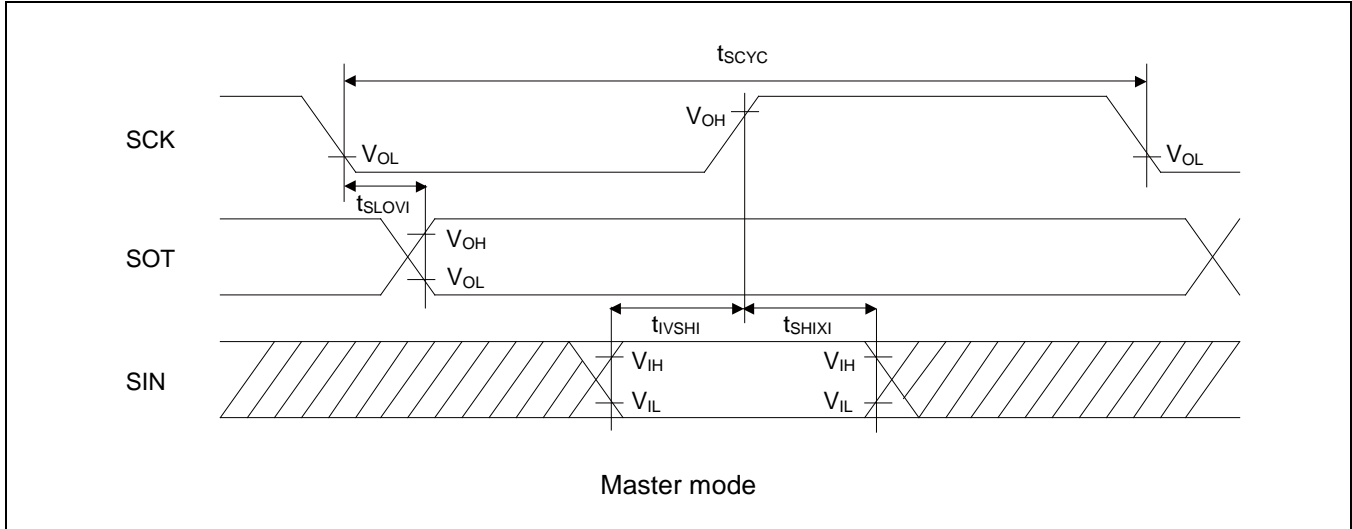
**CSIO (SPI=0, SCINV=0)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4 t_{CYCP}$	-	$4 t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		60	-	50	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx	Slave mode	$2 t_{CYCP} - 10$	-	$2 t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

- The above AC characteristics are for clock synchronous mode.
- $t_{CYCP}$  represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance  $C_L=30\text{ pF}$



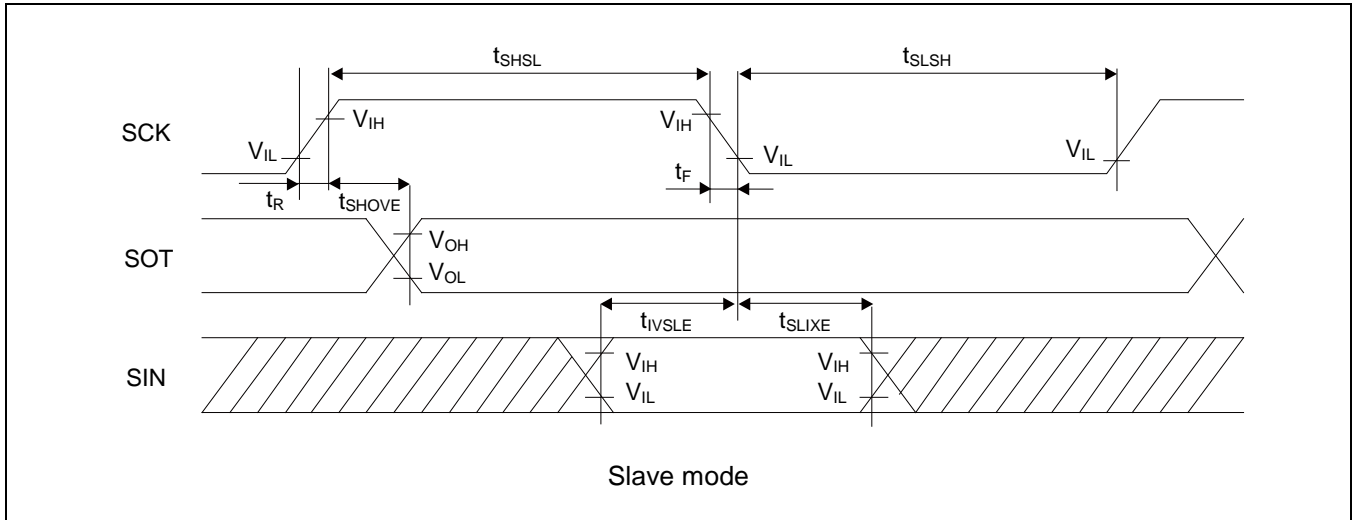
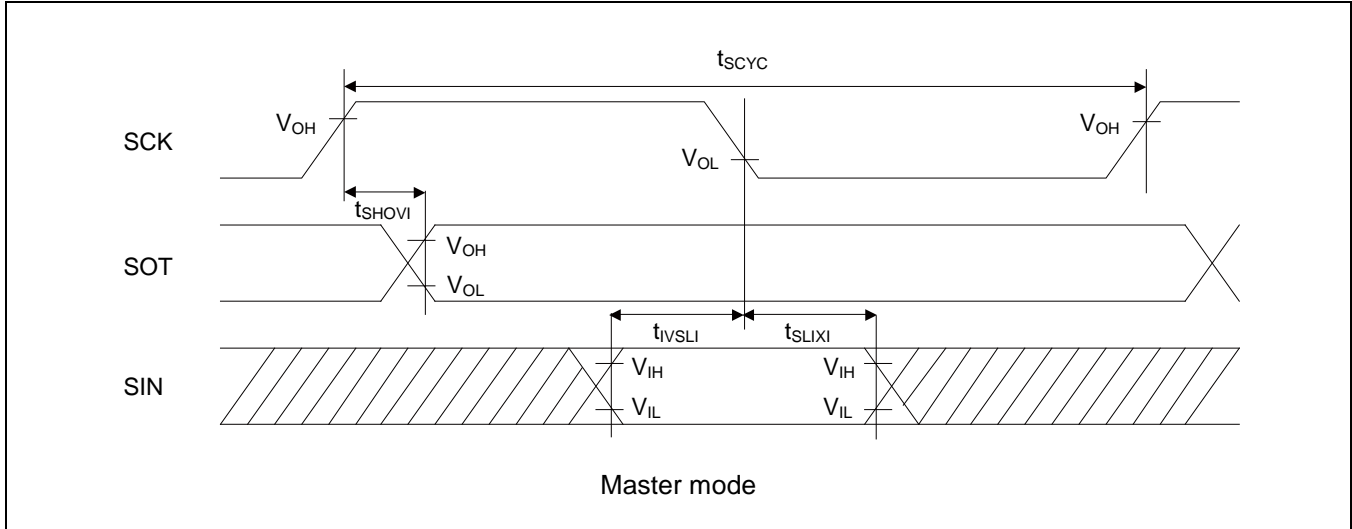
**CSIO (SPI=0, SCINV=1)**

 (V<sub>CC</sub>=AV<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCKx	Master mode	4 t <sub>CYCP</sub>	-	4 t <sub>CYCP</sub>	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN → SCK ↓ setup time	t <sub>IVSLI</sub>	SCKx, SINx		60	-	50	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXI</sub>	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t <sub>SLSH</sub>	SCKx	Slave mode	2 t <sub>CYCP</sub> - 10	-	2 t <sub>CYCP</sub> - 10	-	ns
Serial clock H pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CYCP</sub> + 10	-	t <sub>CYCP</sub> + 10	-	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCKx, SINx		10	-	10	-	ns
SCK ↓ → SIN hold time	t <sub>SLIXE</sub>	SCKx, SINx		20	-	20	-	ns
SCK falling time	t <sub>F</sub>	SCKx		-	5	-	5	ns
SCK rising time	t <sub>R</sub>	SCKx		-	5	-	5	ns

**Notes:**

- The above AC characteristics are for clock synchronous mode.
- t<sub>CYCP</sub> represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance C<sub>L</sub>=30 pF





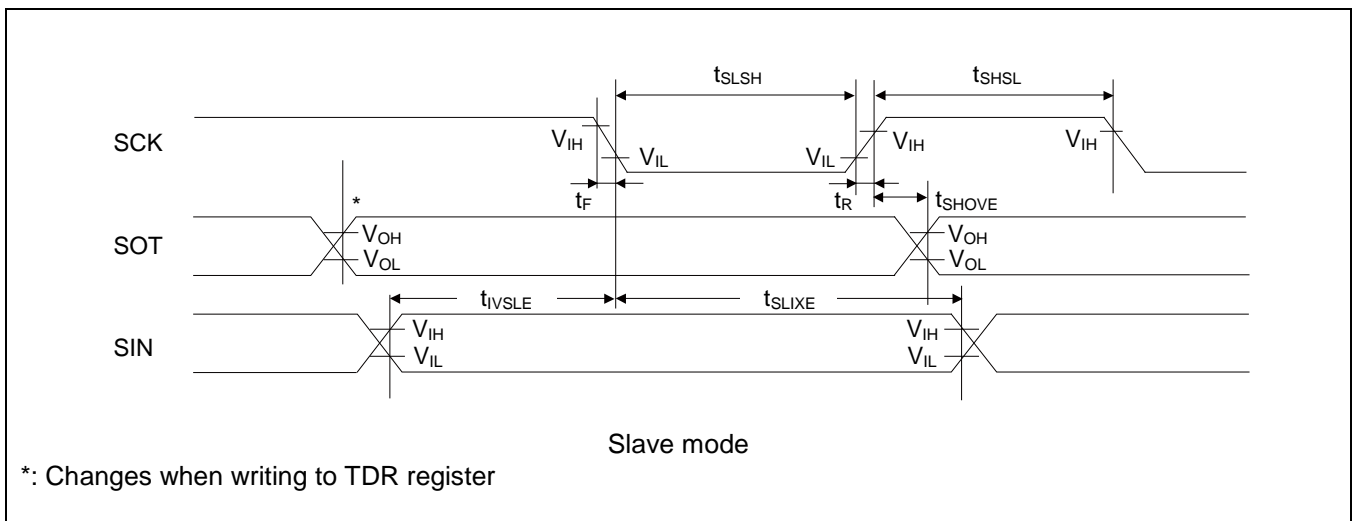
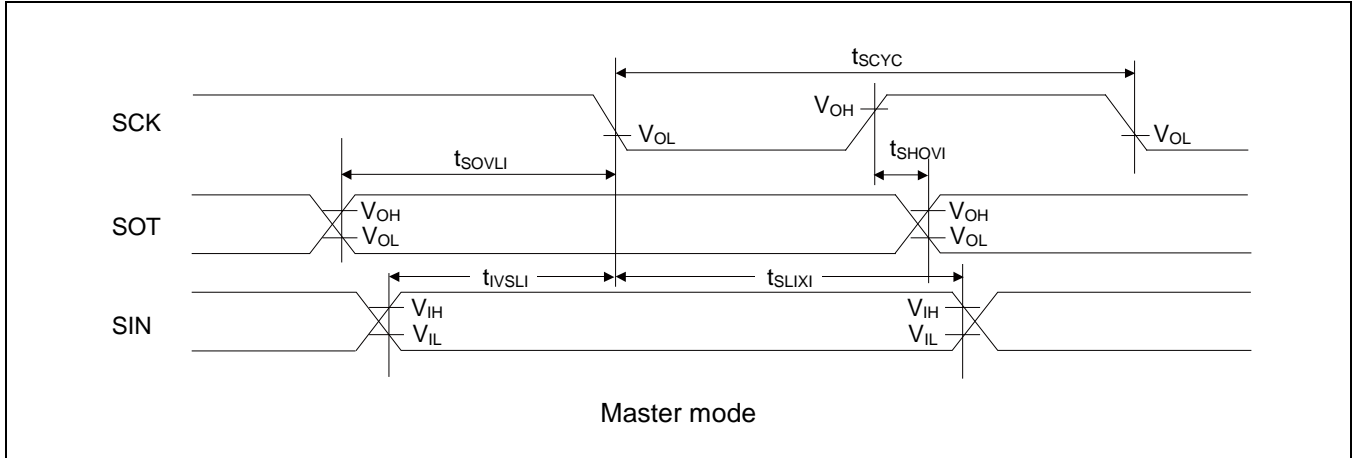
**SPI (SPI=1, SCINV=0)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4 t_{CYCP}$	-	$4 t_{CYCP}$	-	ns
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVI}$	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLI}$	SCKx, SINx		60	-	50	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXI}$	SCKx, SINx		0	-	0	-	ns
SOT $\rightarrow$ SCK $\downarrow$ delay time	$t_{SOVLI}$	SCKx, SOTx		$2 t_{CYCP} - 30$	-	$2 t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx		$2 t_{CYCP} - 10$	-	$2 t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx	$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns	
SCK $\uparrow$ $\rightarrow$ SOT delay time	$t_{SHOVE}$	SCKx, SOTx	Slave mode	-	65	-	52	ns
SIN $\rightarrow$ SCK $\downarrow$ setup time	$t_{IVSLE}$	SCKx, SINx		10	-	10	-	ns
SCK $\downarrow$ $\rightarrow$ SIN hold time	$t_{SLIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

- The above AC characteristics are for clock synchronous mode.
- $t_{CYCP}$  represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance  $C_L=30\text{ pF}$



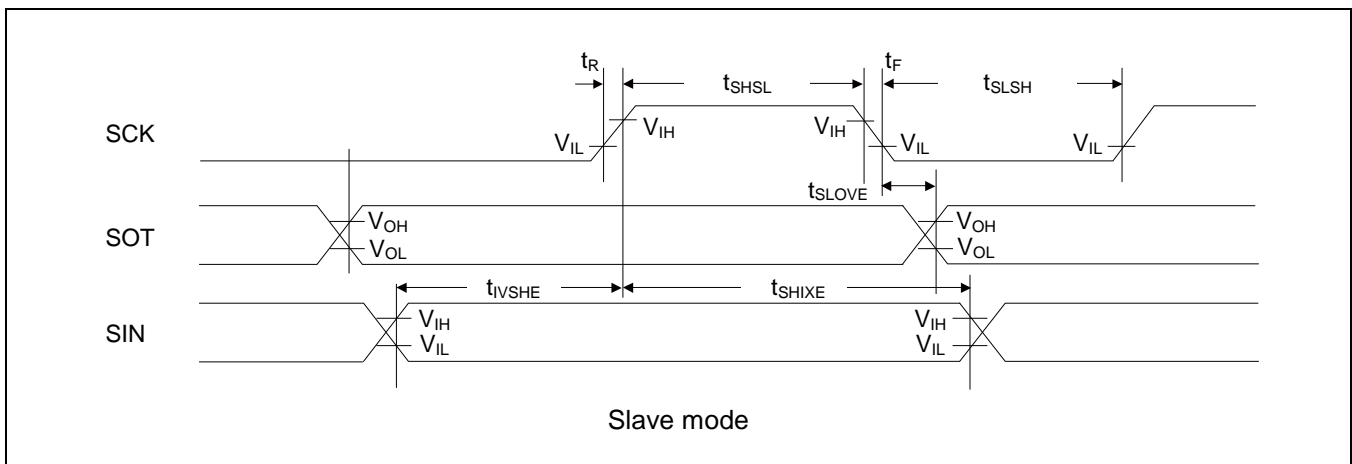
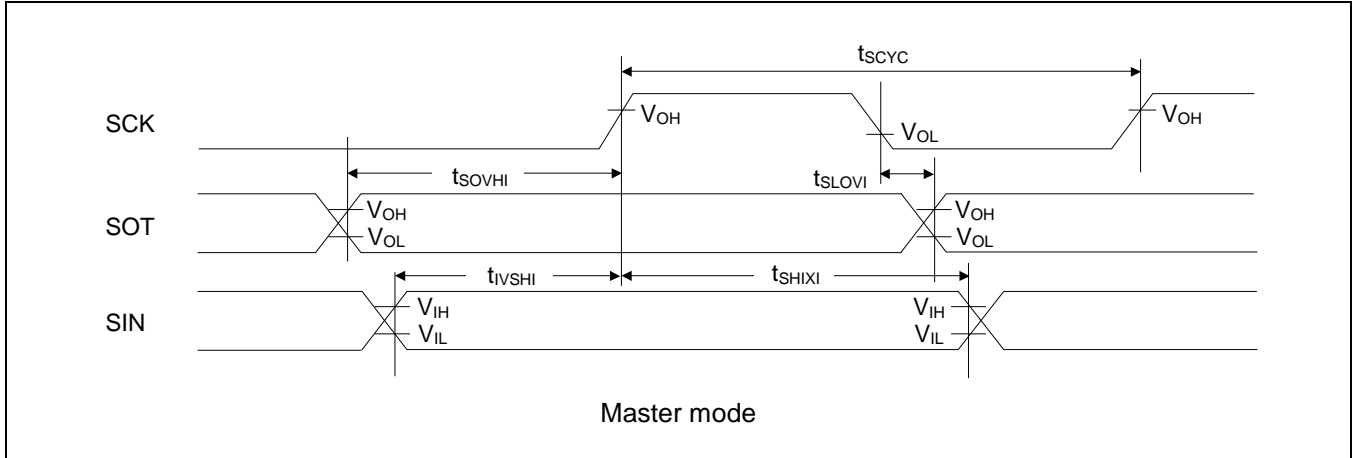
**SPI (SPI=1, SCINV=1)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKx	Master mode	$4 t_{CYCP}$	-	$4 t_{CYCP}$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVI}$	SCKx, SOTx		-30	+30	-20	+20	ns
SIN → SCK ↑ setup time	$t_{IVSHI}$	SCKx, SINx		60	-	50	-	ns
SCK ↑ → SIN hold time	$t_{SHIXI}$	SCKx, SINx		0	-	0	-	ns
SOT → SCK ↑ delay time	$t_{SOVHI}$	SCKx, SOTx		$2 t_{CYCP} - 30$	-	$2 t_{CYCP} - 30$	-	ns
Serial clock L pulse width	$t_{SLSH}$	SCKx	Slave mode	$2 t_{CYCP} - 10$	-	$2 t_{CYCP} - 10$	-	ns
Serial clock H pulse width	$t_{SHSL}$	SCKx		$t_{CYCP} + 10$	-	$t_{CYCP} + 10$	-	ns
SCK ↓ → SOT delay time	$t_{SLOVE}$	SCKx, SOTx		-	65	-	52	ns
SIN → SCK ↑ setup time	$t_{IVSHE}$	SCKx, SINx		10	-	10	-	ns
SCK ↑ → SIN hold time	$t_{SHIXE}$	SCKx, SINx		20	-	20	-	ns
SCK falling time	$t_F$	SCKx		-	5	-	5	ns
SCK rising time	$t_R$	SCKx		-	5	-	5	ns

**Notes:**

- The above AC characteristics are for clock synchronous mode.
- $t_{CYCP}$  represents the APB bus clock cycle time.  
For the number of the APB bus to which Multi-function Serial has been connected, see "8. Block Diagram".
- The characteristics are only applicable when the relocate port numbers are the same.  
For instance, they are not applicable for the combination of SCKx\_0 and SOTx\_1.
- External load capacitance  $C_L=30\text{ pF}$



**When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=1)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
			Min	Max	Min	Max	
SCS $\downarrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	$t_{CSDI}$		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS $\downarrow$ →SCK $\downarrow$ setup time	$t_{CSSE}$	Slave mode	$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCK $\uparrow$ →SCS $\uparrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCS $\downarrow$ →SOT delay time	$t_{DSE}$		-	55	-	43	ns
SCS $\uparrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

\*1: CSSU bit value x serial chip select timing operating clock cycle.

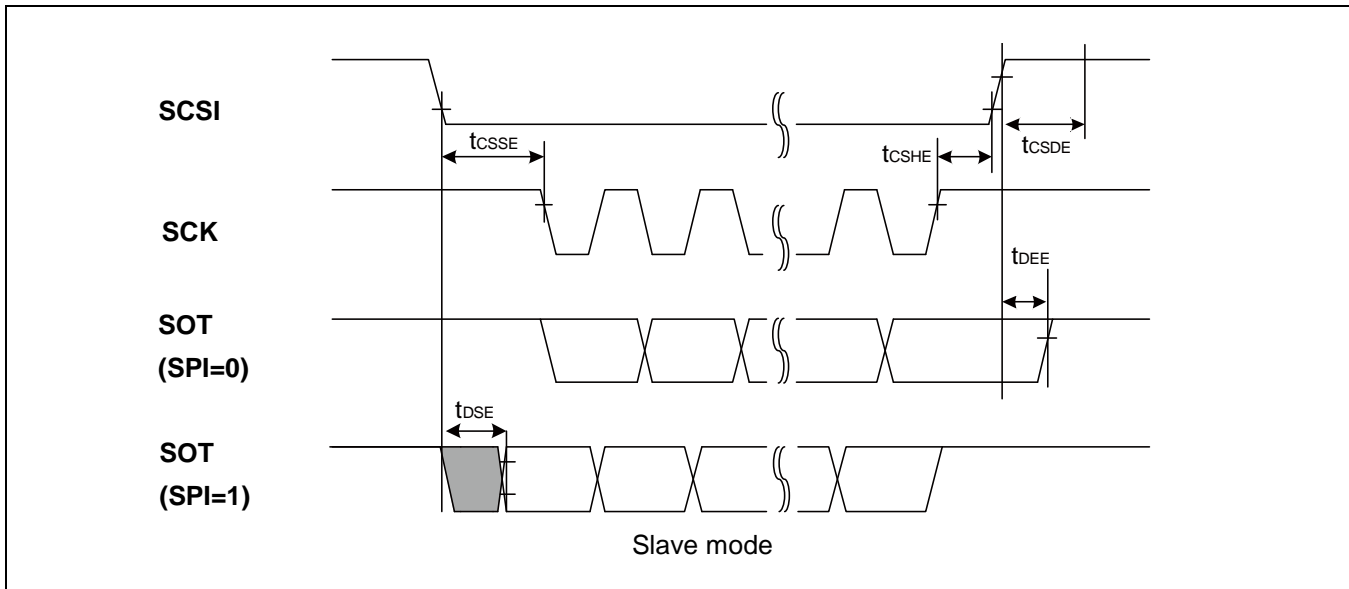
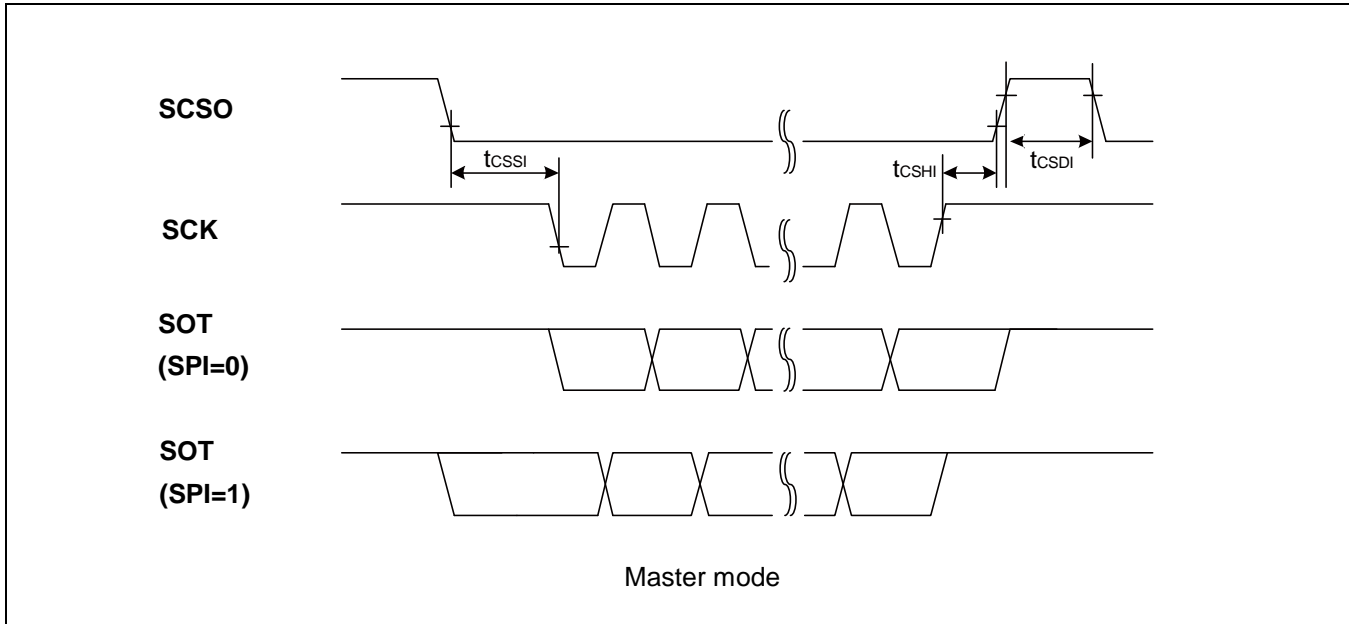
\*2: CSHD bit value x serial chip select timing operating clock cycle.

\*3: CSDS bit value x serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting,  $5t_{CYCP}$  or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

**Notes:**

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance  $C_L=30\text{ pF}$ .



**When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=1)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
			Min	Max	Min	Max	
SCS $\downarrow$ →SCK $\uparrow$ setup time	t <sub>CSSI</sub>	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\downarrow$ →SCS $\uparrow$ hold time	t <sub>CShI</sub>		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t <sub>CSDI</sub>		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS $\downarrow$ →SCK $\uparrow$ setup time	t <sub>CSSe</sub>	Slave mode	3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCK $\downarrow$ →SCS $\uparrow$ hold time	t <sub>CShE</sub>		0	-	0	-	ns
SCS deselect time	t <sub>CSDe</sub>		3t <sub>CYCP</sub> +30	-	3t <sub>CYCP</sub> +30	-	ns
SCS $\downarrow$ →SOT delay time	t <sub>DSE</sub>		-	55	-	43	ns
SCS $\uparrow$ →SOT delay time	t <sub>DEE</sub>		0	-	0	-	ns

\*1: CSSU bit value x serial chip select timing operating clock cycle.

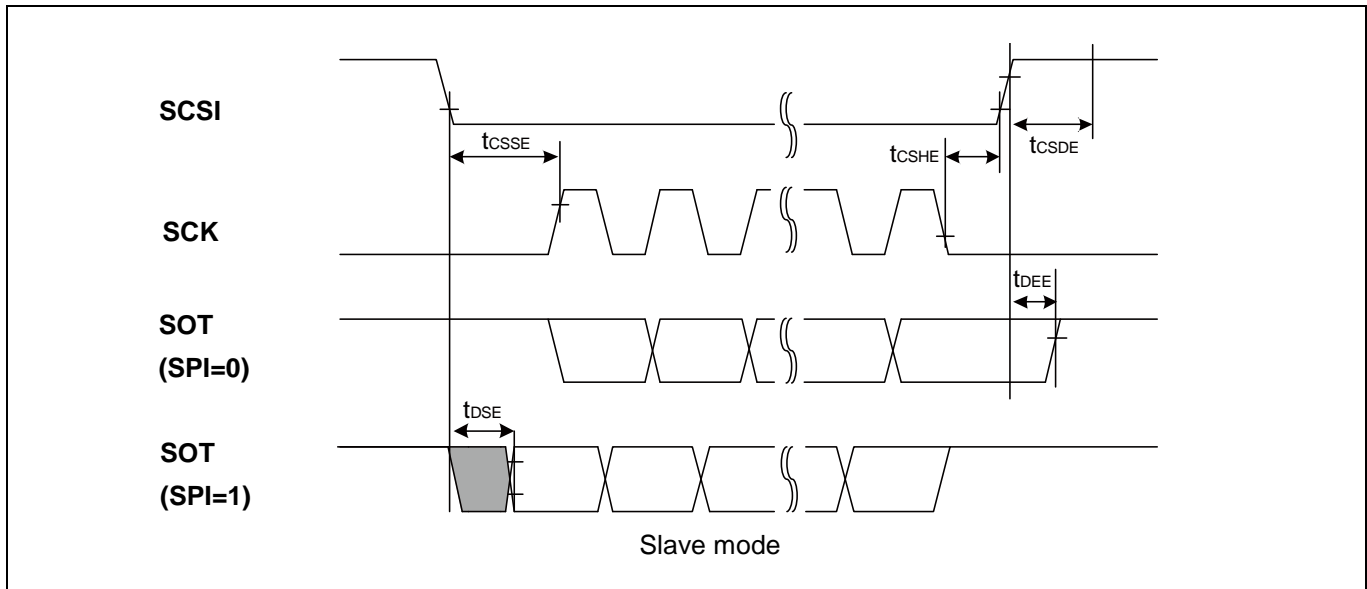
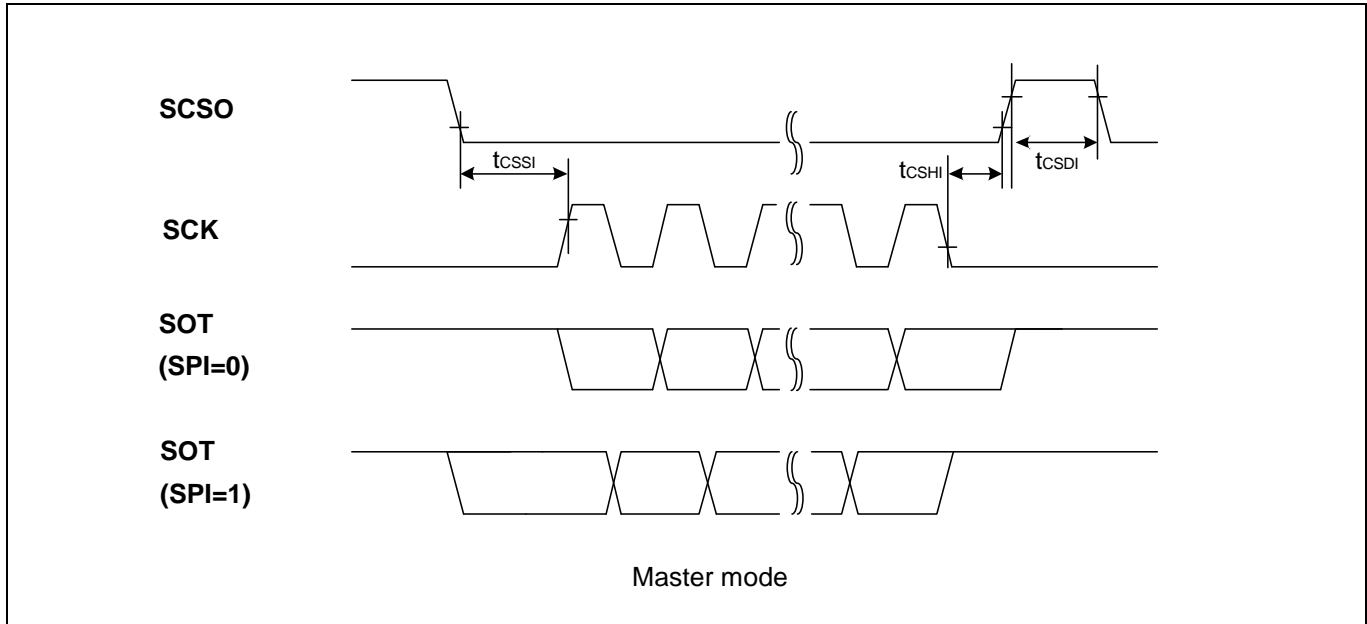
\*2: CSHD bit value x serial chip select timing operating clock cycle.

\*3: CSDS bit value x serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting, 5t<sub>CYCP</sub> or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

**Notes:**

- t<sub>CYCP</sub> indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance C<sub>L</sub>=30 pF.





**When Using CSIO/SPI Chip Select (SCINV=0, CSLVL=0)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
			Min	Max	Min	Max	
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSI}$	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	$t_{CSDI}$		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS $\uparrow$ →SCK $\downarrow$ setup time	$t_{CSSE}$	Slave mode	$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCK $\uparrow$ →SCS $\downarrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCS $\uparrow$ →SOT delay time	$t_{DSE}$		-	55	-	43	ns
SCS $\downarrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

\*1: CSSU bit value x serial chip select timing operating clock cycle.

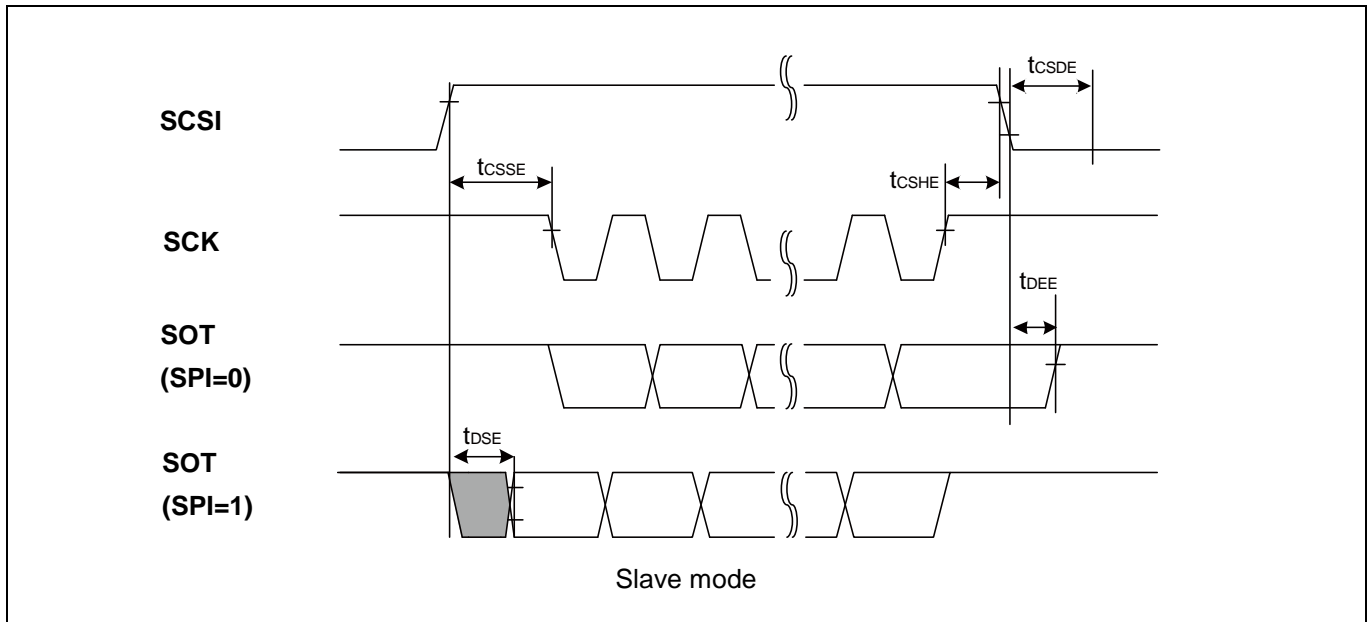
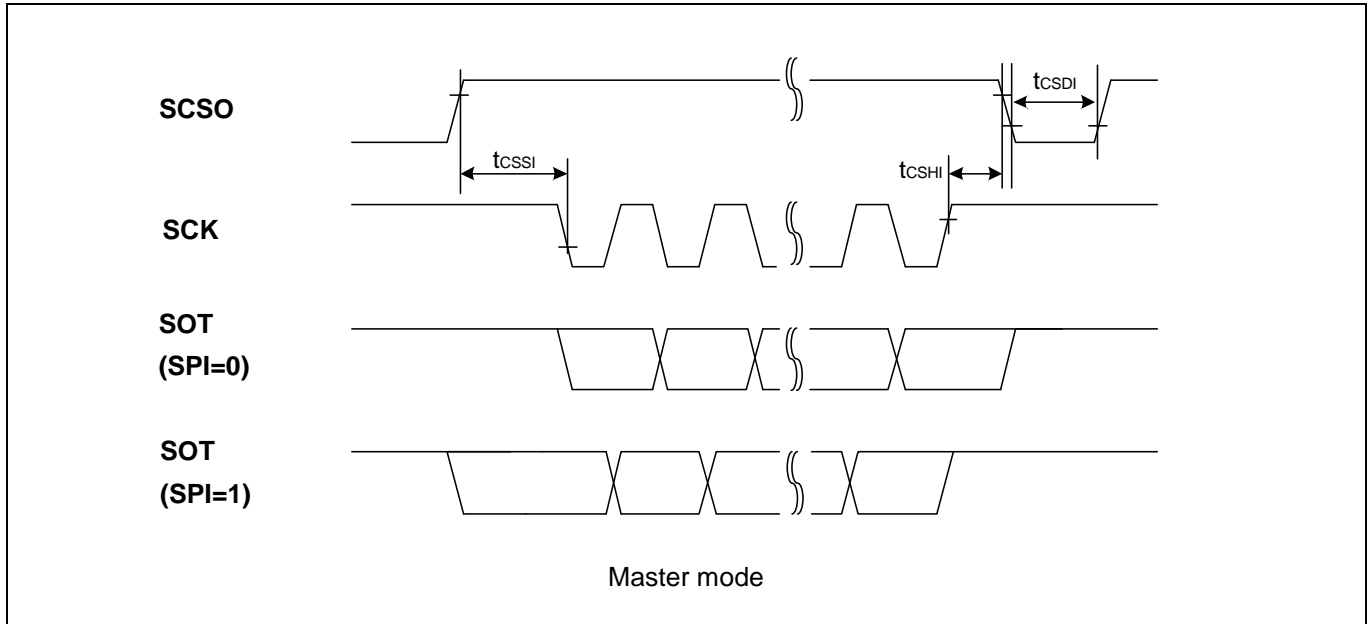
\*2: CSHD bit value x serial chip select timing operating clock cycle.

\*3: CSDS bit value x serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting,  $5t_{CYCP}$  or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

**Notes:**

- $t_{CYCP}$  indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information About CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance  $C_L=30\text{ pF}$ .



**When Using CSIO/SPI Chip Select (SCINV=1, CSLVL=0)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	$V_{CC} < 2.7\text{ V}$		$V_{CC} \geq 2.7\text{ V}$		Unit
			Min	Max	Min	Max	
SCS $\uparrow$ →SCK $\uparrow$ setup time	$t_{CSSI}$	Master mode	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK $\downarrow$ →SCS $\downarrow$ hold time	$t_{CSHI}$		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	$t_{CSDI}$		(*3)-50	(*3)+50	(*3)-50	(*3)+50	ns
SCS $\uparrow$ →SCK $\uparrow$ setup time	$t_{CSSE}$	Slave mode	$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCK $\downarrow$ →SCS $\downarrow$ hold time	$t_{CSHE}$		0	-	0	-	ns
SCS deselect time	$t_{CSDE}$		$3t_{CYCP}+30$	-	$3t_{CYCP}+30$	-	ns
SCS $\uparrow$ →SOT delay time	$t_{DSE}$		-	55	-	43	ns
SCS $\downarrow$ →SOT delay time	$t_{DEE}$		0	-	0	-	ns

\*1: CSSU bit value x serial chip select timing operating clock cycle.

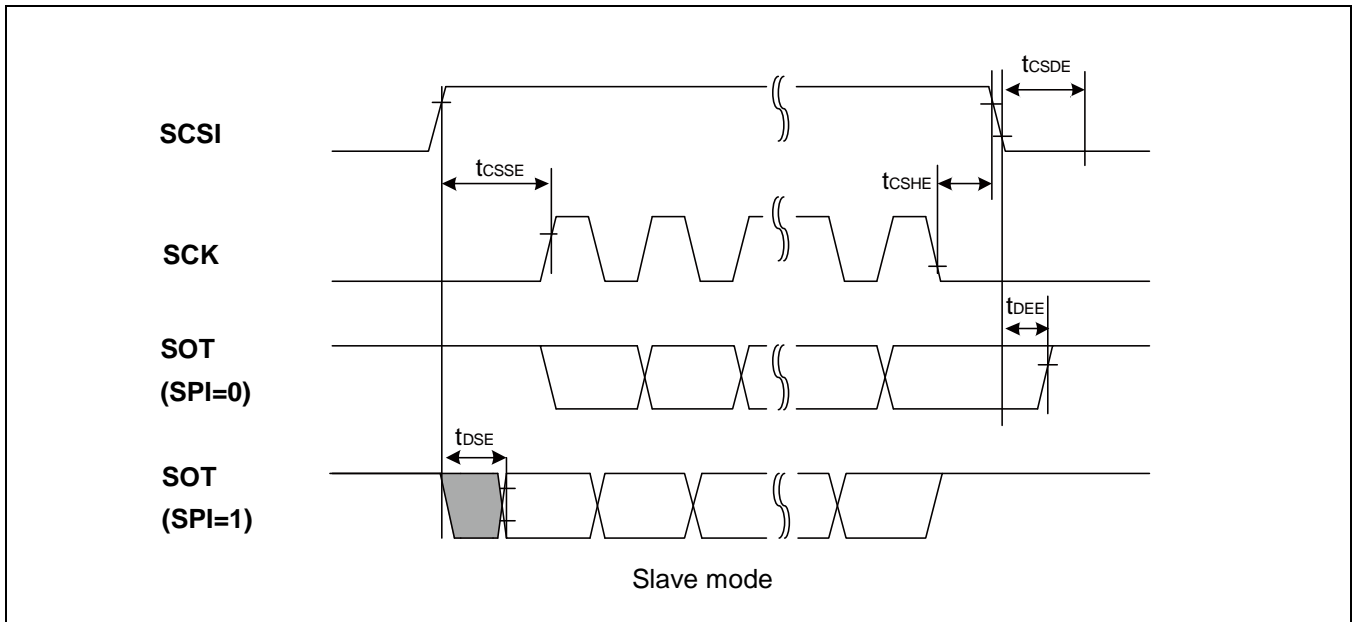
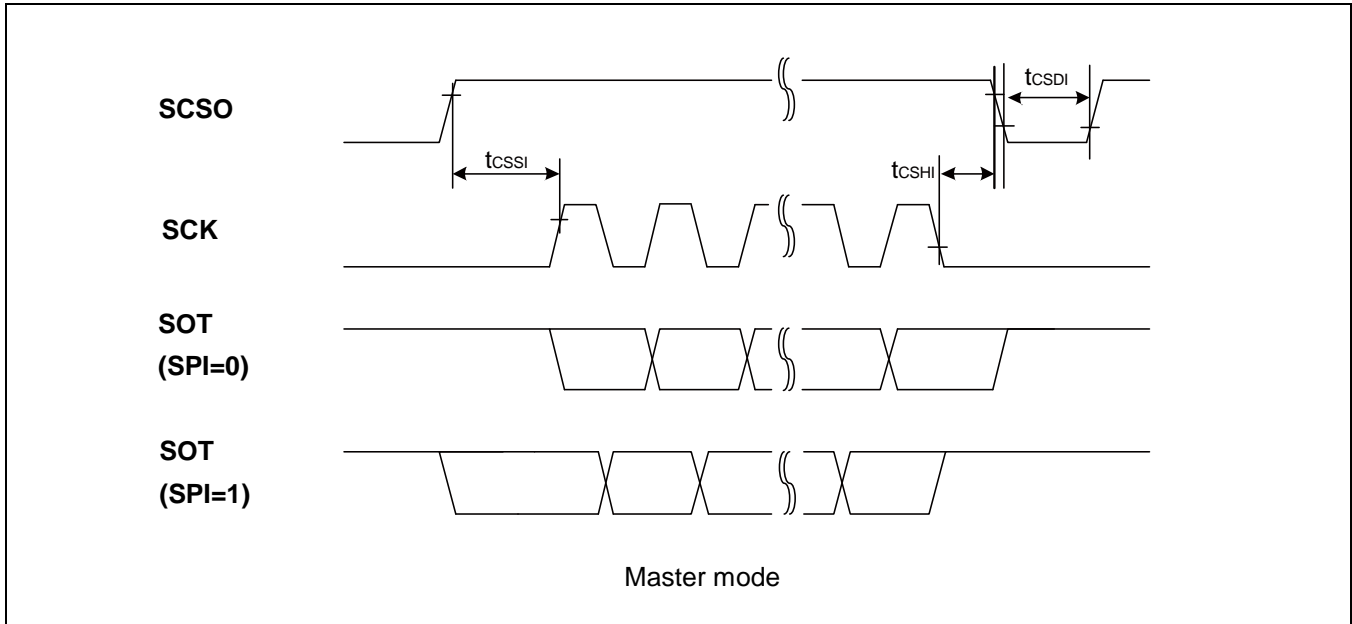
\*2: CSHD bit value x serial chip select timing operating clock cycle.

\*3: CSDS bit value x serial chip select timing operating clock cycle.

Irrespective of CSDS bit setting,  $5t_{CYCP}$  or more are required for the period the time when the serial chip select pin becomes inactive to the time when the serial chip select pin becomes active again.

**Notes:**

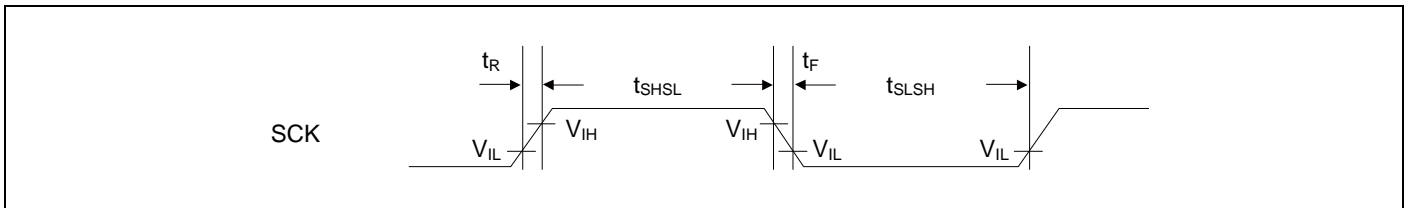
- $t_{CYCP}$  indicates the APB bus clock cycle time.  
For information about the APB bus number which Multi-function Serial is connected to, see "8. Block Diagram".
- For information about CSSU, CSHD, CSDS, serial chip select timing operating clock, see "FM0+ Family Peripheral Manual".
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKx\_0 and SCSIx\_1 is not guaranteed.
- When the external load capacitance  $C_L=30\text{ pF}$ .



**UART external clock input (EXT=1)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Serial clock L pulse width	$t_{SLSH}$	$C_L=30\text{ pF}$	$t_{CYCP} +10$	-	ns	
Serial clock H pulse width	$t_{SHSL}$		$t_{CYCP} +10$	-	ns	
SCK falling time	$t_F$		-	5	ns	
SCK rising time	$t_R$		-	5	ns	



**11.4.10 External Input Timing**

 ( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks				
				Min	Max						
Input pulse width	$t_{INH}$ , $t_{INL}$	ADTGx	-	$2 t_{CYCP}^{*1}$	-	ns	A/D converter trigger input				
		FRCKx					Free-run timer input clock				
		ICxx					Input capture				
		DTTixX					Wave form generator				
		INTxx, NMIX					*2	$2 t_{CYCP} + 100^{*1}$	-	ns	External interrupt, NMI
							*3	500	-	ns	
WKUPx	*4	500	-	ns	Deep standby wake up						

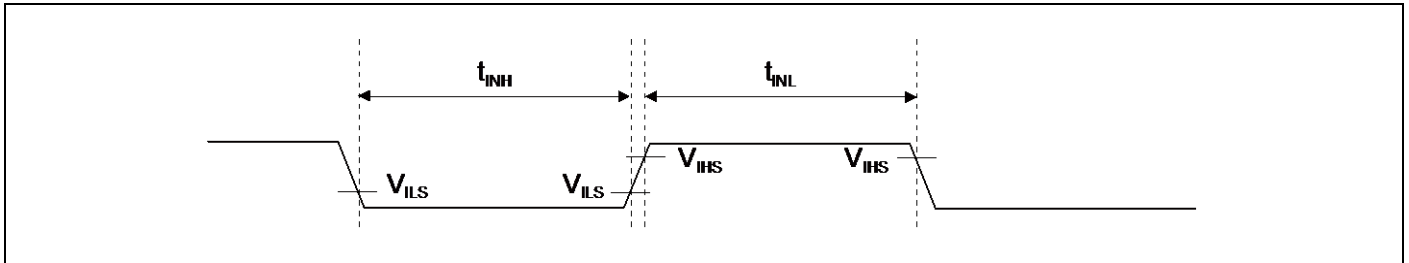
\*1:  $t_{CYCP}$  represents the APB bus clock cycle time.

For the number of the APB bus to which the Multi-function Timer is connected and that of the APB bus to which the External Interrupt Controller is connected, see "8. Block Diagram".

\*2: In Run mode and Sleep mode

\*3: In Timer mode and RTC mode and Stop mode

\*4: In Deep Standby RTC mode and Deep Standby Stop mode

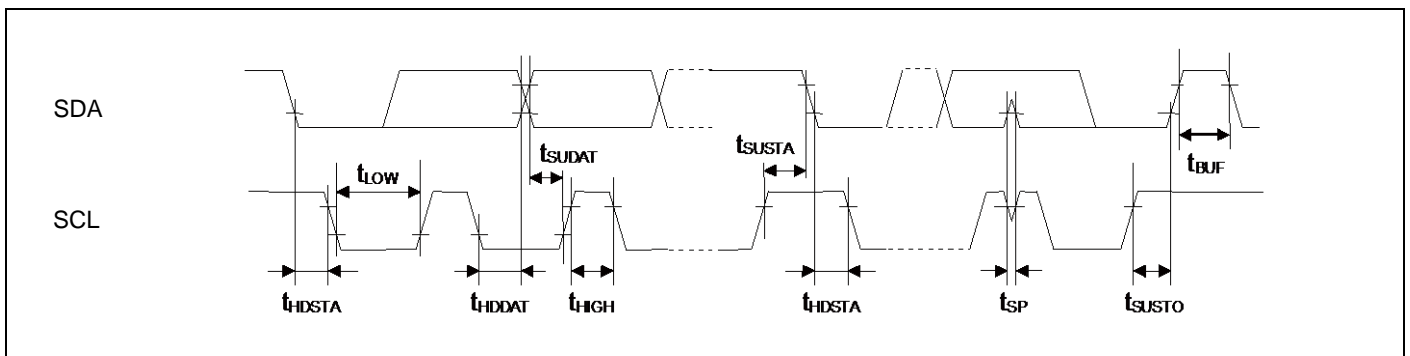


**11.4.11 I<sup>2</sup>C Timing**

(V<sub>CC</sub>=AV<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	Standard-Mode		Fast-Mode		Unit	Remarks
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	C <sub>L</sub> =30 pF, R=(V <sub>P</sub> /I <sub>OL</sub> )* <sup>1</sup>	0	100	0	400	kHz	
(Repeated) Start condition hold time SDA ↓ → SCL ↓	t <sub>HDSTA</sub>		4.0	-	0.6	-	μs	
SCL clock L width	t <sub>LOW</sub>		4.7	-	1.3	-	μs	
SCL clock H width	t <sub>HIGH</sub>		4.0	-	0.6	-	μs	
(Repeated) Start setup time SCL ↑ → SDA ↓	t <sub>SUSTA</sub>		4.7	-	0.6	-	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HDDAT</sub>		0	3.45* <sup>2</sup>	0	0.9* <sup>3</sup>	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SUDAT</sub>		250	-	100	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SUSTO</sub>		4.0	-	0.6	-	μs	
Bus free time between Stop condition and Start condition	t <sub>BUF</sub>		4.7	-	1.3	-	μs	
Noise filter	t <sub>SP</sub>		-	2 t <sub>CYCP</sub> * <sup>4</sup>	-	2 t <sub>CYCP</sub> * <sup>4</sup>	ns	

- \*1: R represents the pull-up resistance of the SCL and SDA lines, and C<sub>L</sub> the load capacitance of the SCL and SDA lines. V<sub>P</sub> represents the power supply voltage of the pull-up resistance, and I<sub>OL</sub> the V<sub>OL</sub> guaranteed current.
- \*2: The maximum t<sub>HDDAT</sub> must satisfy at least the condition that the period during which the device is holding the SCL signal at L (t<sub>LOW</sub>) does not extend.
- \*3: A Fast-mode I<sup>2</sup>C bus device can be used in a Standard-mode I<sup>2</sup>C bus system, provided that the condition of t<sub>SUDAT</sub> ≥ 250 ns is fulfilled.
- \*4: t<sub>CYCP</sub> represents the APB bus clock cycle time.  
For the number of the APB bus to which the I<sup>2</sup>C is connected, see "8. Block Diagram".  
To use Standard-mode, set the APB bus clock at 2 MHz or more.  
To use Fast-mode, set the APB bus clock at 8 MHz or more.

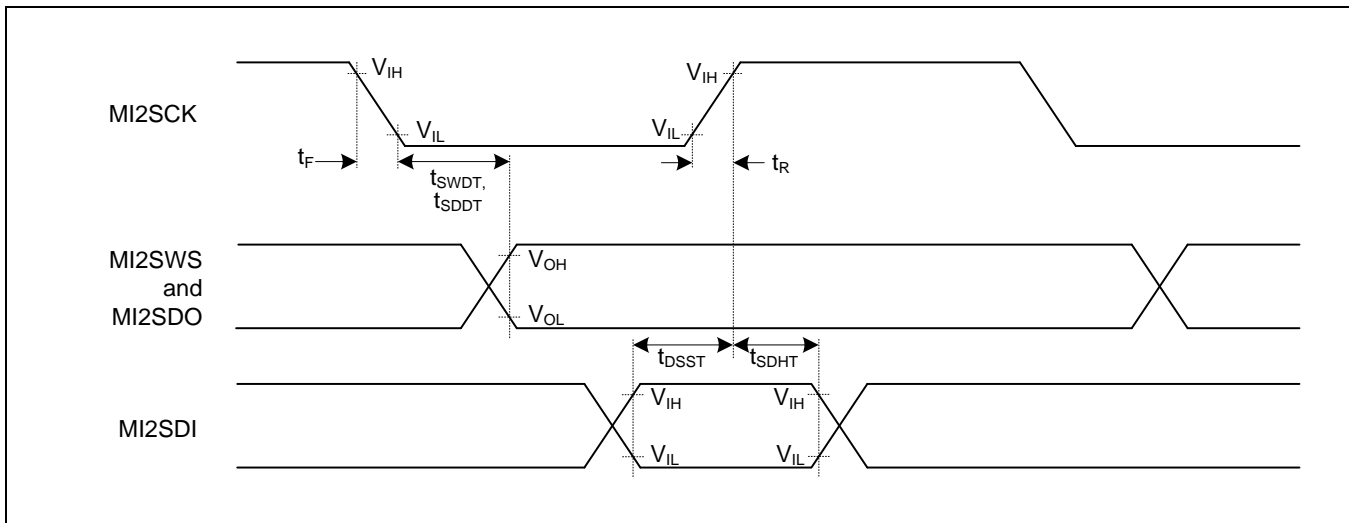


**11.4.12 I<sup>2</sup>S Timing**

(V<sub>CC</sub>=AV<sub>CC</sub>=1.65 V to 3.6 V, V<sub>SS</sub>=AV<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	V <sub>CC</sub> < 2.7 V		V <sub>CC</sub> ≥ 2.7 V		Unit
				Min	Max	Min	Max	
MI2SCK max frequency* <sup>1</sup>	f <sub>MI2SCK</sub>	MI2SCKx	C <sub>L</sub> =30 pF	-	6.144	-	6.144	MHz
I <sup>2</sup> S clock cycle time* <sup>1</sup>	t <sub>ICYC</sub>	MI2SCKx		4 t <sub>CYCP</sub>	-	4 t <sub>CYCP</sub>	-	ns
I <sup>2</sup> S clock Duty cycle	Δ	MI2SCKx		45%	55%	45%	55%	
MI2SCK ↓ → MI2SWS delay time	t <sub>SWDT</sub>	MI2SCKx, MI2SWSx		-30	+30	-20	+20	ns
MI2SCK ↓ → MI2SDO delay time	t <sub>SDDT</sub>	MI2SCKx, MI2SDOx		-30	+30	-20	+20	ns
MI2SDI → MI2SCK ↑ setup time	t <sub>DSST</sub>	MI2SCKx, MI2SDIx		50	-	36	-	ns
MI2SCK ↑ → MI2SDI hold time	t <sub>SDHT</sub>	MI2SCKx, MI2SDIx		0	-	0	-	ns
MI2SCK falling time	t <sub>F</sub>	MI2SCKx		-	5	-	5	ns
MI2SCK rising time	t <sub>R</sub>	MI2SCKx		-	5	-	5	ns

\*1: I<sup>2</sup>S clock should meet the multiple of PCLK (t<sub>ICYC</sub>) and the frequency less than f<sub>MI2SCK</sub> meantime. The detail information please refer to Chapter I<sup>2</sup>S of Communication Macro Part of Peripheral Manual.





**11.4.13 Smart Card Interface Characteristics**

 (V<sub>CC</sub>=1.65 V to 3.3 V, V<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output rising time	t <sub>R</sub>	ICx_VCC, ICx_RST,	C <sub>L</sub> =30 pF	4	20	ns	
Output falling time	t <sub>F</sub>	ICx_CLK, ICx_DATA		4	20	ns	
Output clock frequency	f <sub>CLK</sub>	ICx_CLK		-	20	MHz	
Duty cycle	Δ			45%	55%		

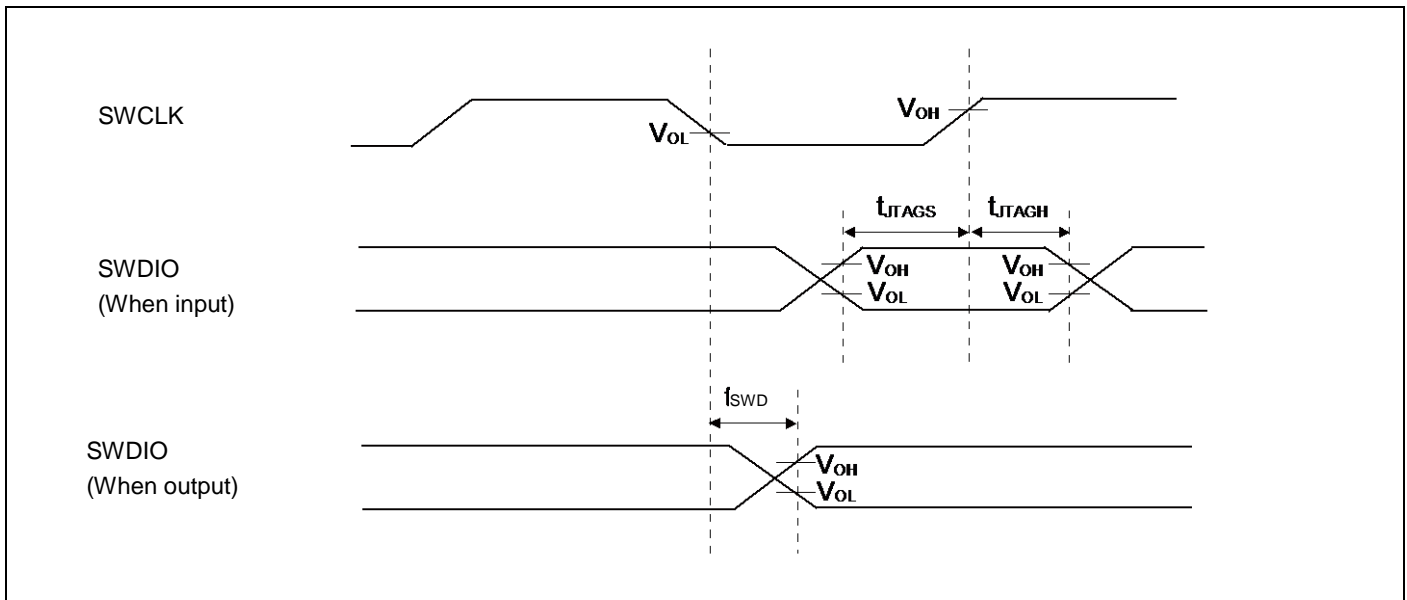
■ External pull-up resistor (20 kΩ to 50 kΩ) must be applied to ICx\_CIN pin when it's used as smart card reader function.

**11.4.14 SW-DP Timing**

 ( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
SWDIO setup time	$t_{SWS}$	SWCLK, SWDIO	-	15	-	ns	
SWDIO hold time	$t_{SWH}$	SWCLK, SWDIO	-	15	-	ns	
SWDIO delay time	$t_{SWD}$	SWCLK, SWDIO	-	-	45	ns	

**Note:**

 - External load capacitance  $C_L=30\text{ pF}$ 


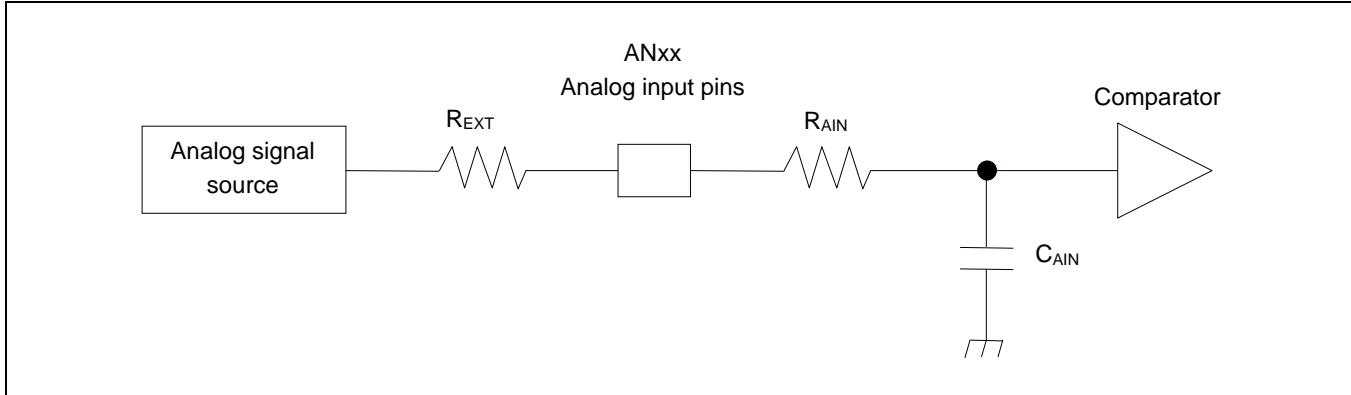
**11.5 12-bit A/D Converter**

**Electrical Characteristics of A/D Converter (Preliminary Values)**

( $V_{CC}=AV_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $V_{SS}=AV_{SS}=0\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral Nonlinearity	-	-	- 4.5	-	4.5	LSB	
Differential Nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	$V_{ZT}$	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	$V_{FST}$	ANxx	AVRH - 15	-	AVRH + 15	mV	
Conversion time *1	-	-	2.0	-	-	$\mu\text{s}$	$AV_{CC} \geq 2.7\text{ V}$
			4.0	-	-		$1.8 \leq AV_{CC} < 2.7\text{ V}$
			10	-	-		$1.65 \leq AV_{CC} < 1.8\text{ V}$
Sampling time *2	$t_s$	-	0.6	-	-	$\mu\text{s}$	$AV_{CC} \geq 2.7\text{ V}$
			1.2	-	10		$1.8 \leq AV_{CC} < 2.7\text{ V}$
			3.0	-	-		$1.65 \leq AV_{CC} < 1.8\text{ V}$
Compare clock cycle *3	$t_{CCK}$	-	100	-	-	ns	$AV_{CC} \geq 2.7\text{ V}$
			200	-	1000		$1.8 \leq AV_{CC} < 2.7\text{ V}$
			500	-	-		$1.65 \leq AV_{CC} < 1.8\text{ V}$
State transition time to operation permission	$t_{STT}$	-	-	-	1.0	$\mu\text{s}$	
Analog input capacity	$C_{AIN}$	-	-	-	9.7	pF	
Analog input resistance	$R_{AIN}$	-	-	-	2.2	k $\Omega$	$AV_{CC} \geq 2.7\text{ V}$
					5.5		$1.8 \leq AV_{CC} < 2.7\text{ V}$
					10.5		$1.65 \leq AV_{CC} < 1.8\text{ V}$
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	$\mu\text{A}$	
Analog input voltage	-	ANxx	$AV_{SS}$	-	AVRH	V	
Reference voltage	-	AVRH	2.7	-	$AV_{CC}$	V	$AV_{CC} \geq 2.7\text{ V}$
			$AV_{CC}$				$AV_{CC} < 2.7\text{ V}$

- \*1: The conversion time is the value of sampling time ( $t_s$ ) + compare time ( $t_c$ ).  
 The minimum conversion time is computed according to the following conditions:  
 $AV_{CC} \geq 2.7\text{ V}$                       sampling time=0.6  $\mu\text{s}$ , compare time=1.4  $\mu\text{s}$   
 $1.8 \leq AV_{CC} < 2.7\text{ V}$               sampling time=1.2  $\mu\text{s}$ , compare time=2.8  $\mu\text{s}$   
 $1.65 \leq AV_{CC} < 1.8\text{ V}$             sampling time=3.0  $\mu\text{s}$ , compare time=7.0  $\mu\text{s}$   
 Ensure that the conversion time satisfies the specifications of the sampling time ( $t_s$ ) and compare clock cycle ( $t_{CCK}$ ).  
 For details of the settings of the sampling time and compare clock cycle, refer to "Chapter: A/D Converter" in "FM0+ Family Peripheral Manual Analog Macro Part".  
 The register settings of the A/D Converter are reflected in the operation according to the APB bus clock timing.  
 For the number of the APB bus to which the A/D Converter is connected, see "8. Block Diagram".  
 The base clock (HCLK) is used to generate the sampling time and the compare clock cycle.
- \*2: The required sampling time varies according to the external impedance.  
 Set a sampling time that satisfies (Equation 1).
- \*3: The compare time ( $t_c$ ) is the result of (Equation 2).



(Equation 1)  $t_S \geq (R_{AIN} + R_{EXT}) \times C_{AIN} \times 9$

t<sub>S</sub>: Sampling time

- R<sub>AIN</sub>:
- Input resistance of A/D Converter = 2.2 kΩ with 2.7 ≤ AV<sub>CC</sub> ≤ 3.6 ch.1 to ch.14, ch.16 to ch.19
  - Input resistance of A/D Converter = 1.9 kΩ with 2.7 ≤ AV<sub>CC</sub> ≤ 3.6 ch.15
  - Input resistance of A/D Converter = 2.3 kΩ with 2.7 ≤ AV<sub>CC</sub> ≤ 3.6 ch.20 to ch.23
  - Input resistance of A/D Converter = 5.7 kΩ with 1.8 ≤ AV<sub>CC</sub> ≤ 2.7 ch.1 to ch.14, ch.16 to ch.19
  - Input resistance of A/D Converter = 5.6 kΩ with 1.8 ≤ AV<sub>CC</sub> ≤ 2.7 ch.15
  - Input resistance of A/D Converter = 5.8 kΩ with 1.8 ≤ AV<sub>CC</sub> ≤ 2.7 ch.20 to ch.23
  - Input resistance of A/D Converter = 12.6 kΩ with 1.65 ≤ AV<sub>CC</sub> ≤ 1.8 ch.1 to ch.19
  - Input resistance of A/D Converter = 12.7 kΩ with 1.65 ≤ AV<sub>CC</sub> ≤ 1.8 ch.20 to ch.23

C<sub>AIN</sub>: Input capacitance of A/D Converter = 9.7 pF with 2.7 ≤ AV<sub>CC</sub> ≤ 3.6

R<sub>EXT</sub>: Output impedance of external circuit

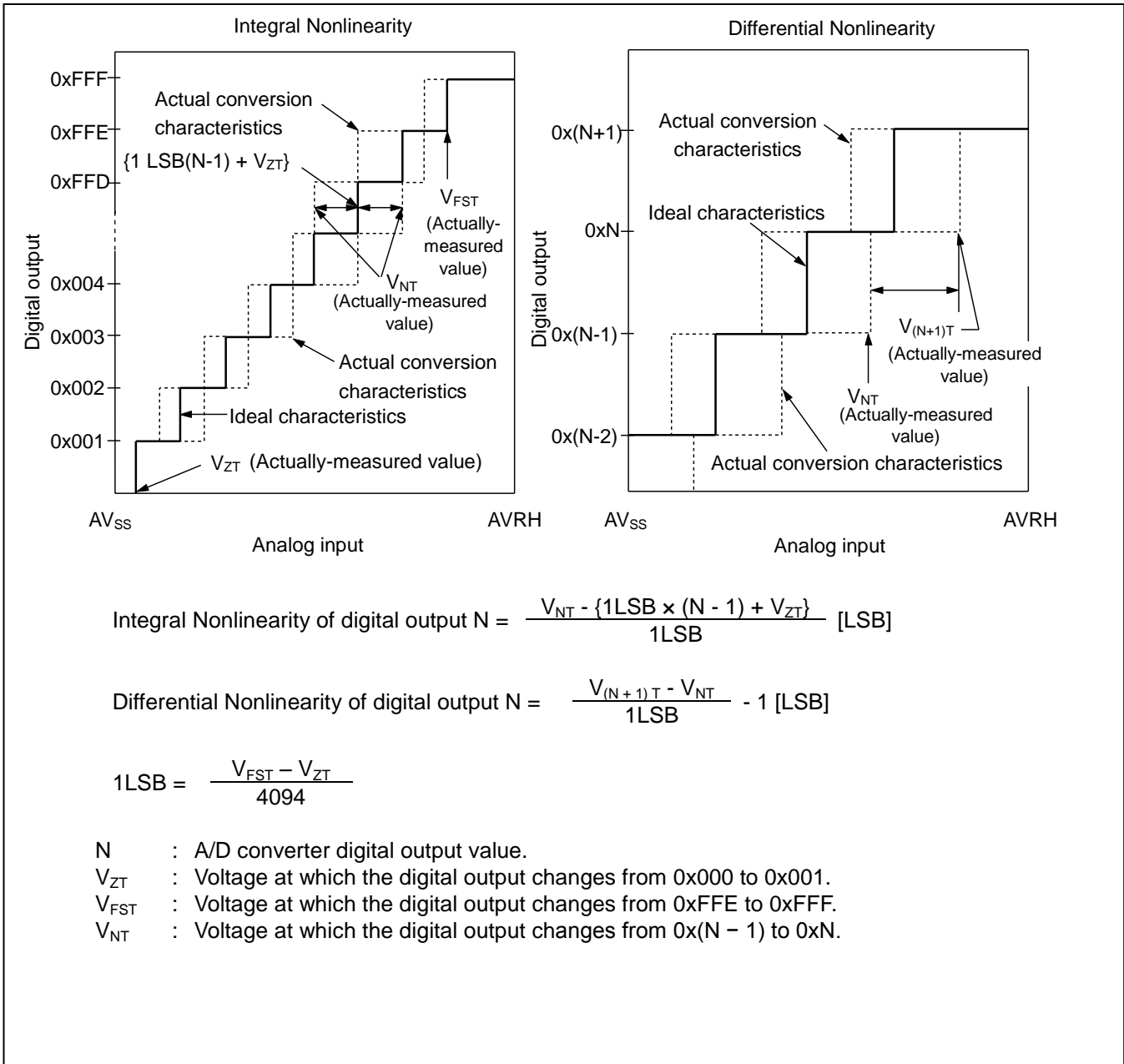
(Equation 2)  $t_C = t_{CCK} \times 14$

t<sub>C</sub>: Compare time

t<sub>CCK</sub>: Compare clock cycle

**Definitions of 12-bit A/D Converter Terms**

- Resolution: Analog variation that is recognized by an A/D converter.
- Integral Nonlinearity: Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- Differential Nonlinearity: Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



**11.6 USB Characteristics**

(V<sub>CC</sub>=3.0 V to 3.6 V, V<sub>SS</sub>=0 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input characteristics	Input H level voltage	V <sub>IH</sub>	-	2.0	V <sub>CC</sub> + 0.3	V	*1
	Input L level voltage	V <sub>IL</sub>	-	V <sub>SS</sub> - 0.3	0.8	V	*1
	Differential input sensitivity	V <sub>DI</sub>	-	0.2	-	V	*2
	Differential common mode range	V <sub>CM</sub>	-	0.8	2.5	V	*2
Output characteristic	Output H level voltage	V <sub>OH</sub>	External pull-down resistance = 15 kΩ	2.8	3.6	V	*3
	Output L level voltage	V <sub>OL</sub>	External pull-up resistance = 1.5 kΩ	0.0	0.3	V	*3
	Crossover voltage	V <sub>CRS</sub>	-	1.3	2.0	V	*4
	Rising time	t <sub>FR</sub>	Full-speed	4	20	ns	*5
	Falling time	t <sub>FF</sub>	Full-speed	4	20	ns	*5
	Rising/Falling time matching	t <sub>FRFM</sub>	Full-speed	90	111.11	%	*5
	Output impedance	Z <sub>DRV</sub>	Full-speed	28	44	Ω	*6
	Rising time	t <sub>LR</sub>	Low-speed	75	300	ns	*7
	Falling time	t <sub>LF</sub>	Low-speed	75	300	ns	*7
	Rising/Falling time matching	t <sub>LRFM</sub>	Low-speed	80	125	%	*7

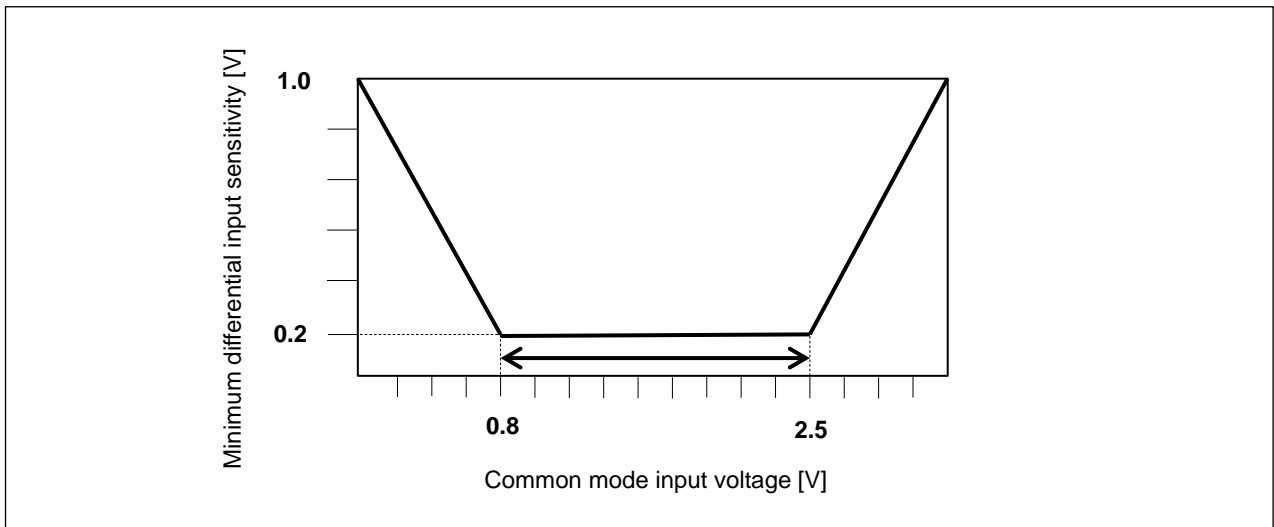
\*1 : The switching threshold voltage of single-end-receiver of USB I/O buffer is set as within V<sub>IL</sub>(Max)=0.8 V, V<sub>IH</sub>(Min)=2.0 V (TTL input standard).

There are some hysteresis to lower noise sensitivity.

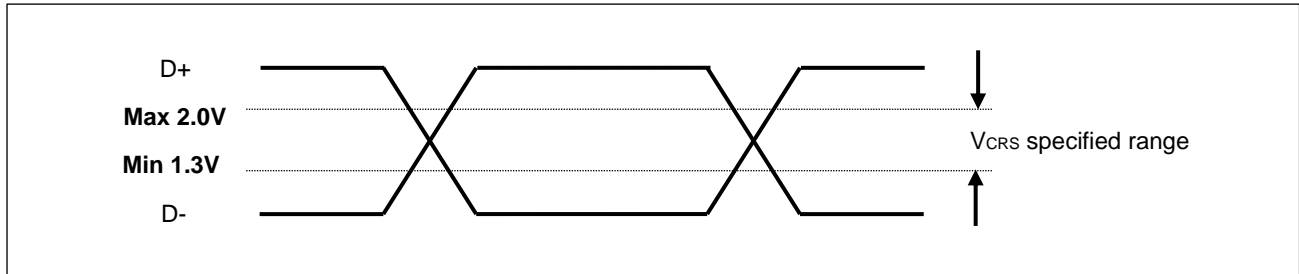
\*2 : Use differential-receiver to receive USB differential data signal.

Differential-receiver has 200 mV of differential input sensitivity when the differential data input is within 0.8 V to 2.5 V to the local ground reference level.

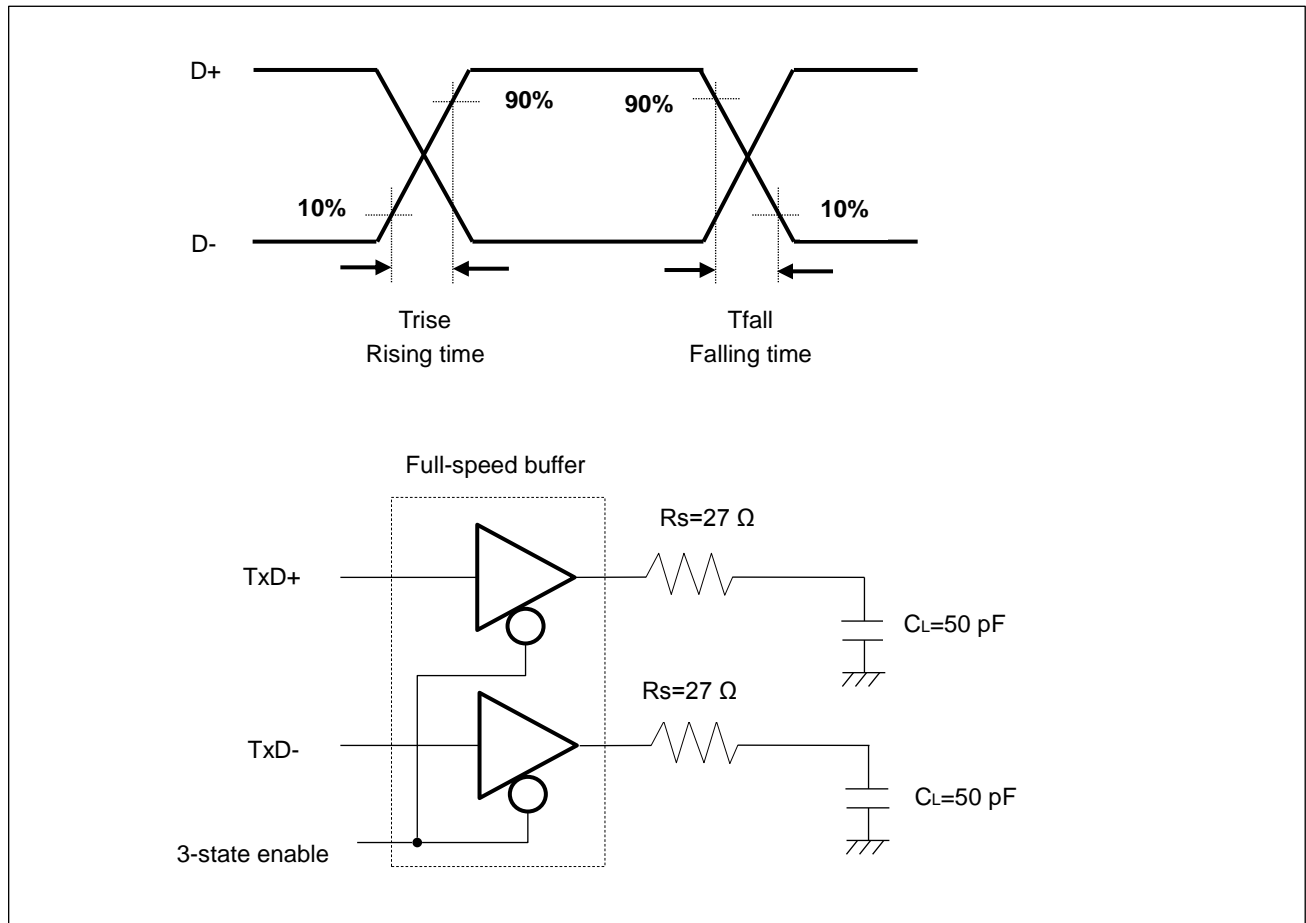
Above voltage range is the common mode input voltage range.



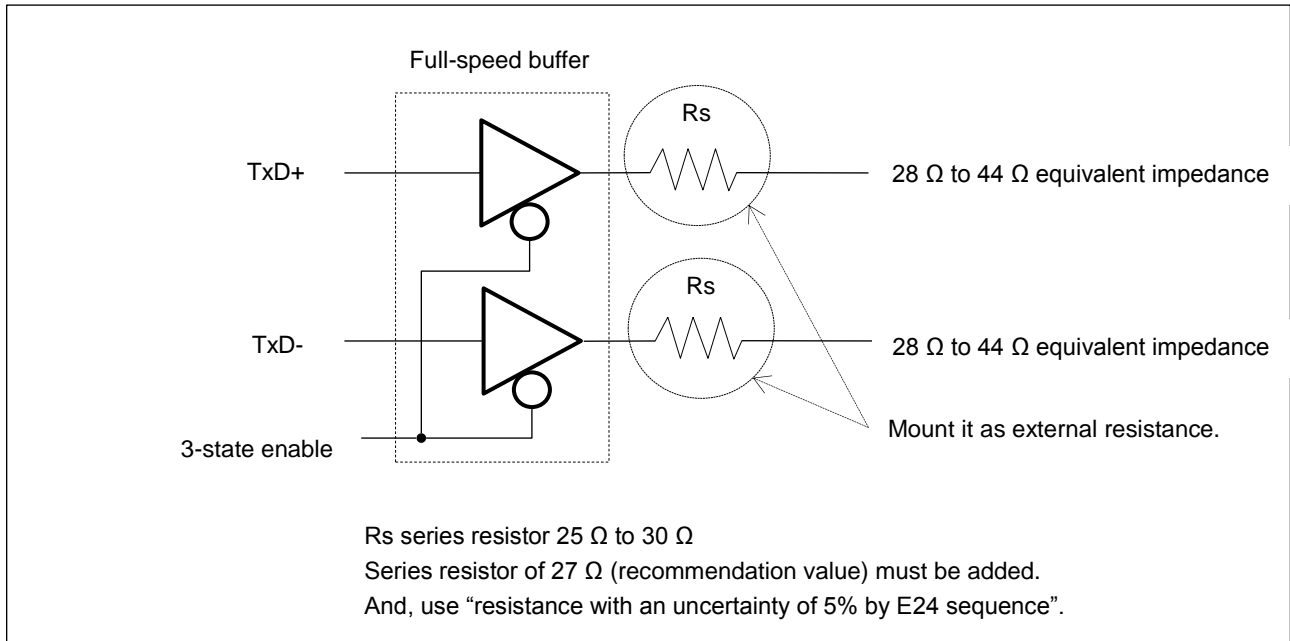
- \*3 : The output drive capability of the driver is below 0.3 V at Low-state ( $V_{OL}$ ) (to 3.6 V and 1.5 k $\Omega$  load), and 2.8 V or above (to the VSS and 1.5 k $\Omega$  load) at high-state ( $V_{OH}$ )
- \*4 : The cross voltage of the external differential output signal (D+ / D-) of USB I/O buffer is within 1.3 V to 2.0 V.



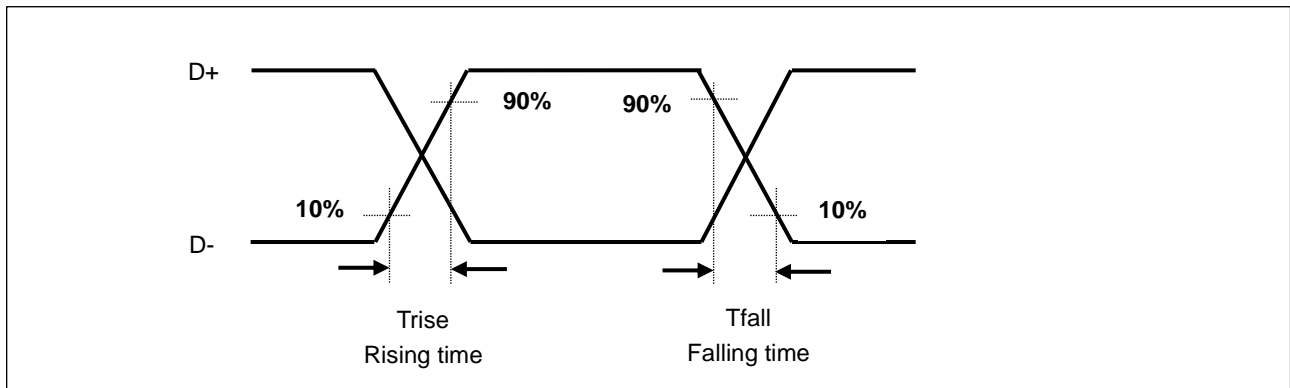
- \*5 : The indicate rising time ( $T_{rise}$ ) and falling time ( $T_{fall}$ ) of the full-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage. For full-speed buffer,  $T_r/T_f$  ratio is regulated as within  $\pm 10\%$  to minimize RFI emission.



- \*6 : USB Full-speed connection is performed via twist pair cable shield with  $90 \Omega \pm 15\%$  characteristic impedance (Differential Mode). USB standard defines that output impedance of USB driver must be in range from  $28\Omega$  to  $44\Omega$ . So, discrete series resistor ( $R_s$ ) addition is defined in order to satisfy the above definition and keep balance. When using this USB I/O, use it with  $25 \Omega$  to  $33 \Omega$  (recommendation value :  $27 \Omega$ ) series resistor  $R_s$ .



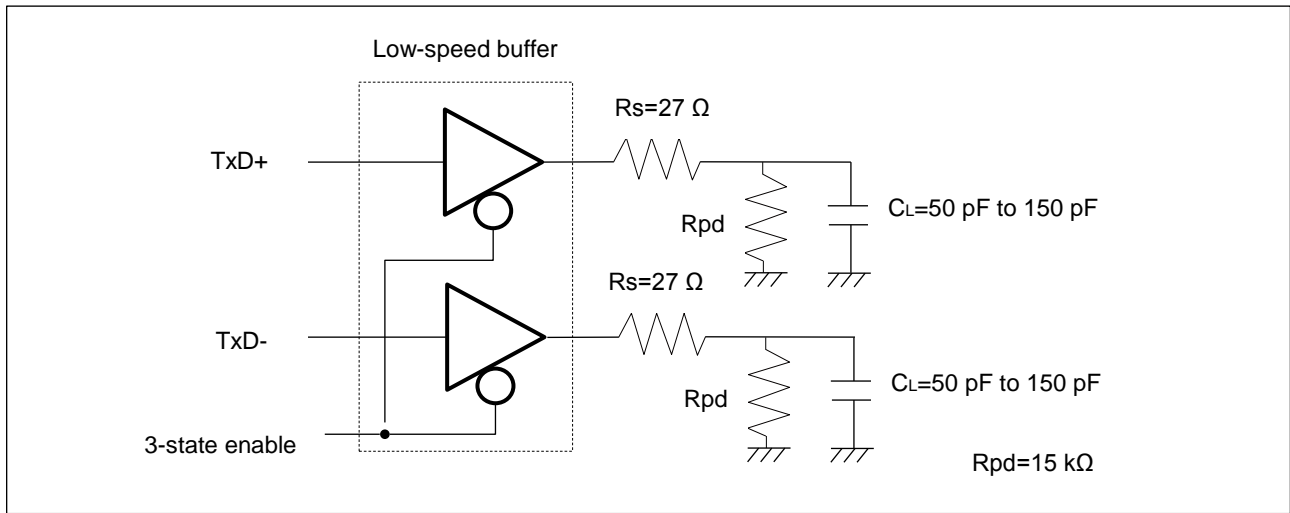
\*7 : They indicate rising time ( $T_{rise}$ ) and falling time ( $T_{fall}$ ) of the low-speed differential data signal. They are defined by the time between 10% and 90% of the output signal voltage.



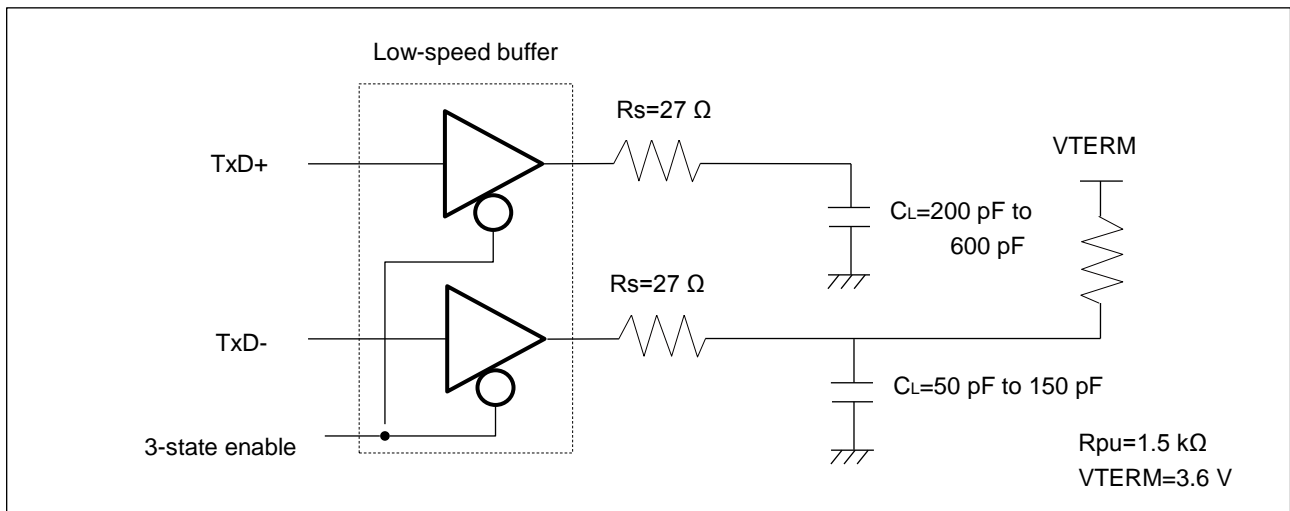
See "Low-speed load (Compliance Load)" for condition of external load.



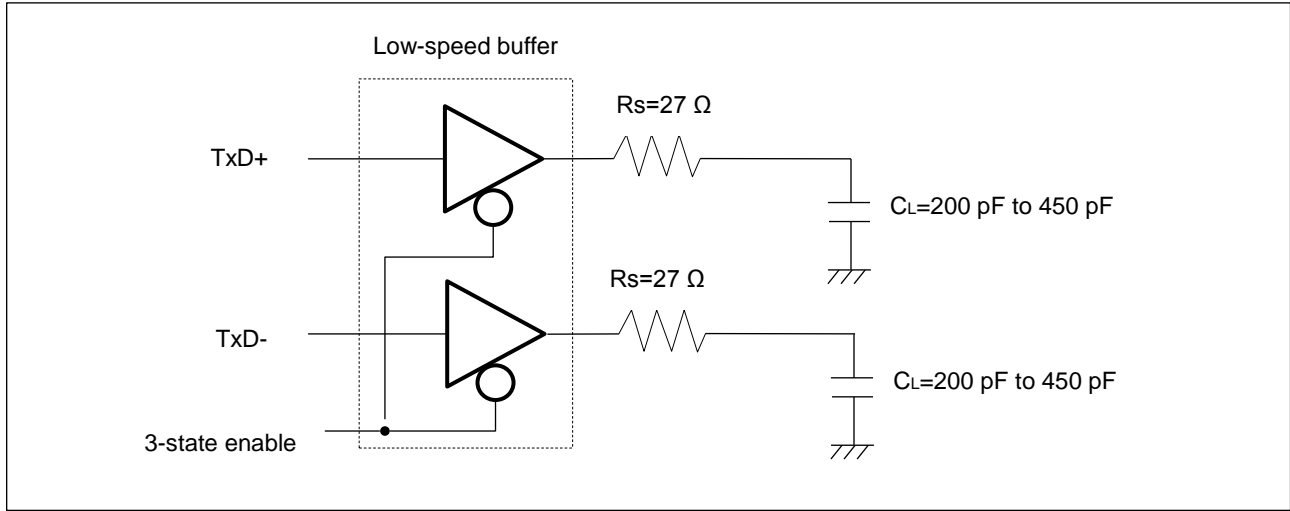
• Low-Speed Load (Upstream Port Load) – Reference 1



• Low-Speed Load (Downstream Port Load) – Reference 2



- Low-Speed Load (Compliance Load)



## 11.7 Low-Voltage Detection Characteristics

### 11.7.1 Low-Voltage Detection Reset

 (T<sub>A</sub>=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	V <sub>DL</sub>	Fixed <sup>*1</sup>	1.38	1.50	1.60	V	When voltage drops
Released voltage	V <sub>DH</sub>		1.43	1.55	1.65	V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	8160x t <sub>CYCP</sub> <sup>*2</sup>	μs	
LVD detection delay time	t <sub>LVDL</sub>	-	-	-	200	μs	

\*1: The value of low voltage detection reset is always fixed.

\*2: t<sub>CYCP</sub> indicates the APB1 bus clock cycle time.

**11.7.2 Low-Voltage Detection Interrupt**

(T<sub>A</sub>=-40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH	SVHRLI=00100	1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVHI=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH	SVHRLI=00101	1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVHI=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH	SVHRLI=00110	1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVHI=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH	SVHRLI=00111	1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVHI=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH	SVHRLI=01000	1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVHI=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH	SVHRLI=01001	1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVHI=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH	SVHRLI=01010	1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVHI=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH	SVHRLI=01011	1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVHI=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH	SVHRLI=01100	2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVHI=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH	SVHRLI=01101	2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVHI=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH	SVHRLI=01110	2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVHI=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH	SVHRLI=01111	2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVHI=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH	SVHRLI=10000	2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVHI=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH	SVHRLI=10001	2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVHI=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH	SVHRLI=10010	2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVHI=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH	SVHRLI=10011	3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	8160 × t <sub>CYCP</sub> *	μs	
LVD detection delay time	t <sub>LVDL</sub>	-	-	-	200	μs	

\*: t<sub>CYCP</sub> represents the APB1 bus clock cycle time.

**11.7.3 Low-Voltage Detection Interrupt 2**

(T<sub>A</sub>=- 40°C to +105°C)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVH2I=00100	1.56	1.70	1.84	V	When voltage drops
Released voltage	VDH	SVH2RLI=00100	1.61	1.75	1.89	V	When voltage rises
Detected voltage	VDL	SVH2I=00101	1.61	1.75	1.89	V	When voltage drops
Released voltage	VDH	SVH2RLI=00101	1.66	1.80	1.94	V	When voltage rises
Detected voltage	VDL	SVH2I=00110	1.66	1.80	1.94	V	When voltage drops
Released voltage	VDH	SVH2RLI=00110	1.70	1.85	2.00	V	When voltage rises
Detected voltage	VDL	SVH2I=00111	1.70	1.85	2.00	V	When voltage drops
Released voltage	VDH	SVH2RLI=00111	1.75	1.90	2.05	V	When voltage rises
Detected voltage	VDL	SVH2I=01000	1.75	1.90	2.05	V	When voltage drops
Released voltage	VDH	SVH2RLI=01000	1.79	1.95	2.11	V	When voltage rises
Detected voltage	VDL	SVH2I=01001	1.79	1.95	2.11	V	When voltage drops
Released voltage	VDH	SVH2RLI=01001	1.84	2.00	2.16	V	When voltage rises
Detected voltage	VDL	SVH2I=01010	1.84	2.00	2.16	V	When voltage drops
Released voltage	VDH	SVH2RLI=01010	1.89	2.05	2.21	V	When voltage rises
Detected voltage	VDL	SVH2I=01011	1.89	2.05	2.21	V	When voltage drops
Released voltage	VDH	SVH2RLI=01011	1.93	2.10	2.27	V	When voltage rises
Detected voltage	VDL	SVH2I=01100	2.30	2.50	2.70	V	When voltage drops
Released voltage	VDH	SVH2RLI=01100	2.39	2.60	2.81	V	When voltage rises
Detected voltage	VDL	SVH2I=01101	2.39	2.60	2.81	V	When voltage drops
Released voltage	VDH	SVH2RLI=01101	2.48	2.70	2.92	V	When voltage rises
Detected voltage	VDL	SVH2I=01110	2.48	2.70	2.92	V	When voltage drops
Released voltage	VDH	SVH2RLI=01110	2.58	2.80	3.02	V	When voltage rises
Detected voltage	VDL	SVH2I=01111	2.58	2.80	3.02	V	When voltage drops
Released voltage	VDH	SVH2RLI=01111	2.67	2.90	3.13	V	When voltage rises
Detected voltage	VDL	SVH2I=10000	2.67	2.90	3.13	V	When voltage drops
Released voltage	VDH	SVH2RLI=10000	2.76	3.00	3.24	V	When voltage rises
Detected voltage	VDL	SVH2I=10001	2.76	3.00	3.24	V	When voltage drops
Released voltage	VDH	SVH2RLI=10001	2.85	3.10	3.35	V	When voltage rises
Detected voltage	VDL	SVH2I=10010	2.85	3.10	3.35	V	When voltage drops
Released voltage	VDH	SVH2RLI=10010	2.94	3.20	3.46	V	When voltage rises
Detected voltage	VDL	SVH2I=10011	2.94	3.20	3.46	V	When voltage drops
Released voltage	VDH	SVH2RLI=10011	3.04	3.30	3.56	V	When voltage rises
LVD stabilization wait time	t <sub>LVDW</sub>	-	-	-	8160 × t <sub>CYCP</sub> *	μs	
LVD detection delay time	t <sub>LVDL</sub>	-	-	-	200	μs	

\*: t<sub>CYCP</sub> represents the APB1 bus clock cycle time.

**11.8 Flash Memory Write/Erase Characteristics**

(V<sub>CC</sub>=1.65 V to 3.6 V, T<sub>A</sub>=- 40°C to +105°C)

Parameter		Value			Unit	Remarks
		Min	Typ*	Max*		
Sector erase time	Large sector	-	1.1	2.7	s	The sector erase time includes the time of writing prior to internal erase.
	Small sector	-	0.3	0.9		
Halfword (16-bit) write time		-	30	528	µs	The halfword (16-bit) write time excludes the system-level overhead.
Chip erase time		-	11.2	28.8	s	The chip erase time includes the time of writing prior to internal erase.

\*: The typical value is immediately after shipment, the maximum value is guarantee value under 10,000 cycle of erase/write.

**Write/Erase Cycle and Data Hold Time (Target Value)**

Write/Erase Cycle	Data Hold Time (Year)	Remarks
1,000	20*	
10,000	10*	

\*: At average + 85°C

**11.9 Return Time from Low-Power Consumption Mode**

**11.9.1 Return Factor: Interrupt/WKUP**

The return time from Low-Power consumption mode is indicated as follows. It is from receiving the return factor to starting the program operation.

**Return Count Time**

( $V_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $T_A=-40^\circ\text{C to }+105^\circ\text{C}$ )

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max <sup>1</sup>		
Sleep mode	t <sub>CNT</sub>	6*HCLK	7*HCLK	μs	
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		12*HCLK	13*HCLK	μs	
Low-speed CR Timer mode		20+12*HCLK	42+13*HCLK	μs	
Sub Timer mode		20+12*HCLK	42+13*HCLK	μs	
RTC mode, Stop mode		38 <sup>(*3)</sup> 38+t <sub>OSCWT</sub> <sup>(*2,4)</sup>	71 71+t <sub>OSCWT</sub> <sup>(*2,4)</sup>	μs	The count time is different in different clock mode
Deep RTC mode, Deep Stop mode		45	80	μs	

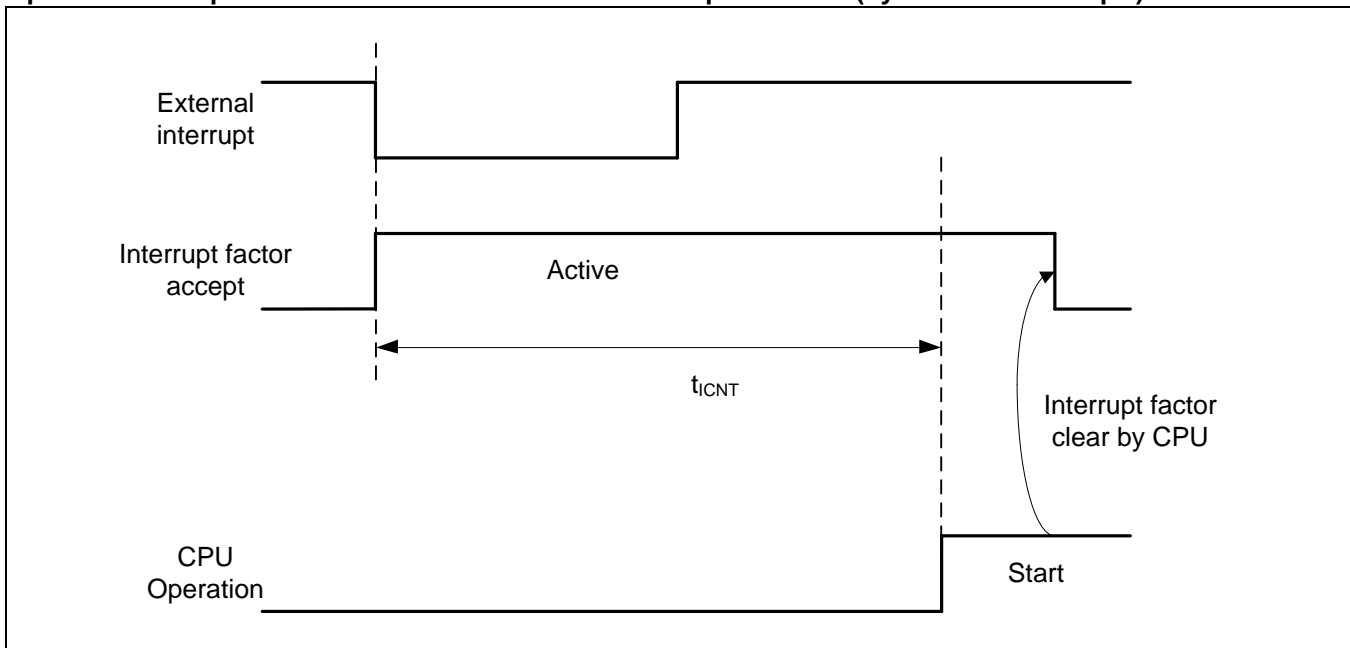
\*1: The maximum value depends on the condition of environment.

\*2: t<sub>OSCWT</sub>: Oscillator stabilization time.

\*3: It is for HCR mode.

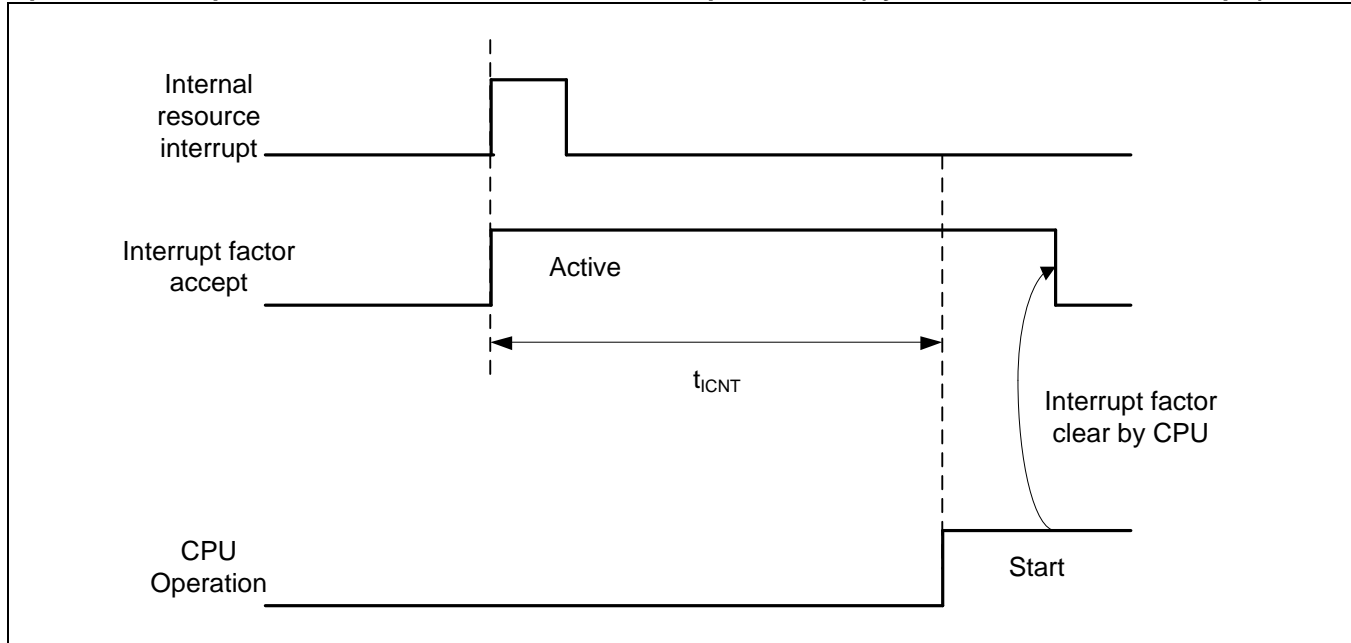
\*4: For clock mode except HCR mode.

**Operation Example of Return from Low-Power Consumption Mode (by External Interrupt\*)**



\*: External interrupt is set to detecting fall edge.

**Operation Example of Return from Low-Power Consumption Mode (by Internal Resource Interrupt\*)**



\*: Internal resource interrupt is not included in return factor by the kind of Low-Power consumption mode.

**Notes:**

- The return factor is different in each Low-Power consumption modes. See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".



**11.9.2 Return Factor: Reset**

The return time from Low-Power consumption mode is indicated as follows. It is from releasing reset to starting the program operation.

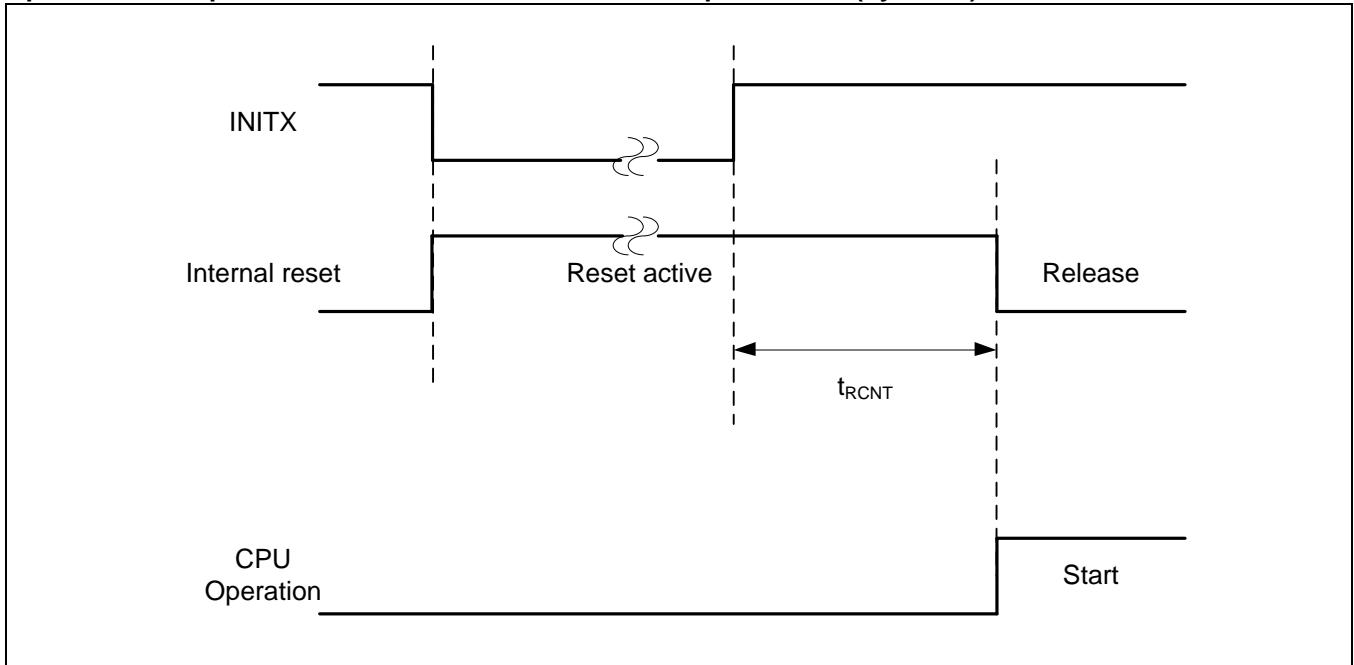
**Return Count Time**

( $V_{CC}=1.65\text{ V to }3.6\text{ V}$ ,  $T_A=-40^{\circ}\text{C to }+105^{\circ}\text{C}$ )

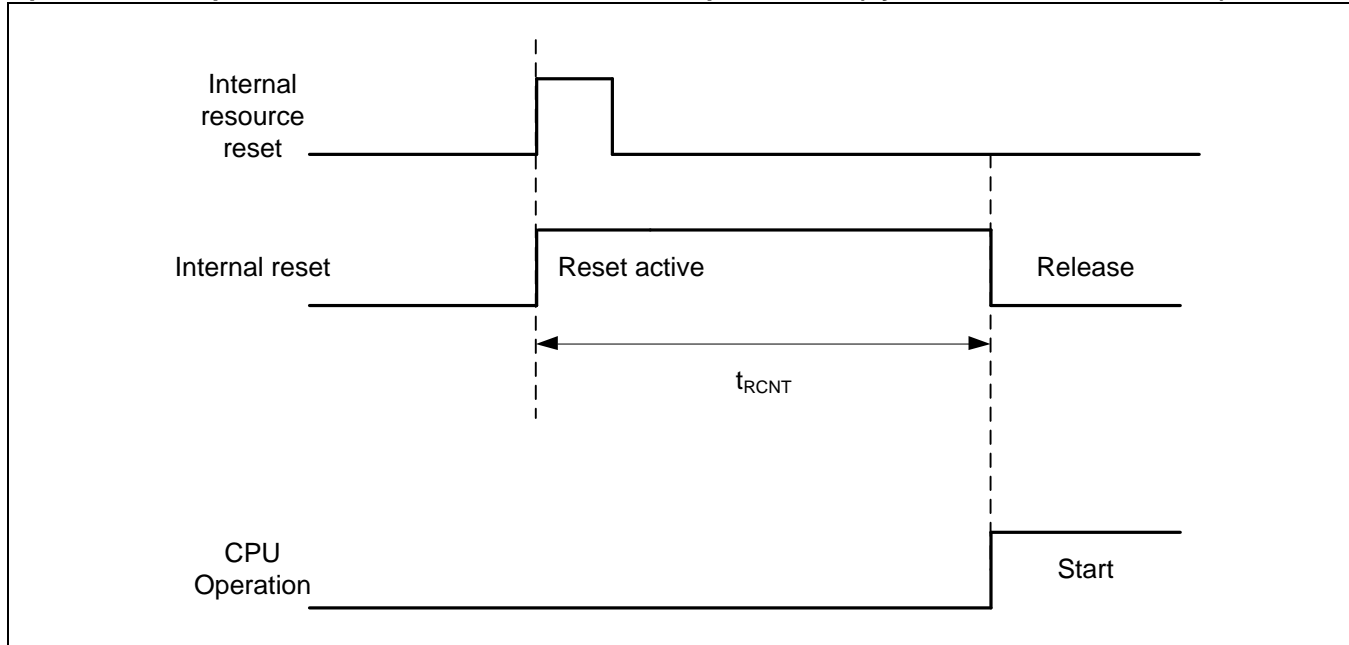
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t <sub>RCNT</sub>	10 <sup>*1</sup> 40 <sup>*2</sup>	70	μs	*1 : HCR ON.(HCR/MOSC/PLL mode) *2 : HCR OFF.(LCR/SOS mode)
High-speed CR Timer mode, Main Timer mode, PLL Timer mode		20	30	μs	
Low-speed CR Timer mode		61	114	μs	
Sub Timer mode		61	114	μs	
RTC/Stop mode		38	85	μs	
Deep RTC mode, Deep Stop mode		46	95	μs	

\*: The maximum value depends on the accuracy of built-in CR.

**Operation Example of Return from Low-Power Consumption Mode (by INITX)**



**Operation Example of Return from Low Power Consumption Mode (by Internal Resource Reset\*)**



\*: Internal resource reset is not included in return factor by the kind of Low-Power consumption mode.

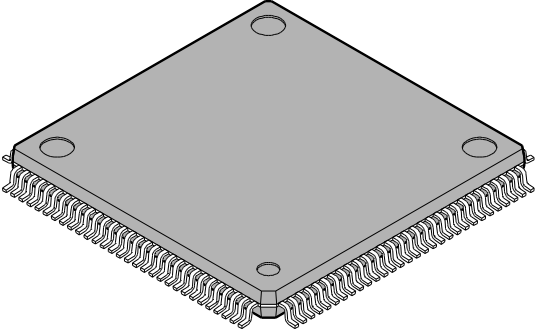
**Notes:**

- The return factor is different in each Low-Power consumption modes. See "Chapter: Low Power Consumption Mode" and "Operations of Standby Modes" in FM0+ Family Peripheral Manual.
- When interrupt recovers, the operation mode that CPU recovers depends on the state before the Low-Power consumption mode transition. See "Chapter: Low Power Consumption Mode" in "FM0+ Family Peripheral Manual".
- The time during the power-on reset/low-voltage detection reset is excluded. See "11.4.7 Power-on Reset Timing in 11.4 AC Characteristics in 11. Electrical Characteristics" for the detail on the time during the power-on reset/low -voltage detection reset.
- When in recovery from reset, CPU changes to the high-speed CR run mode. When using the main clock or the PLL clock, it is necessary to add the main clock oscillation stabilization wait time or the main PLL clock stabilization wait time.
- The internal resource reset means the watchdog reset and the CSV reset.

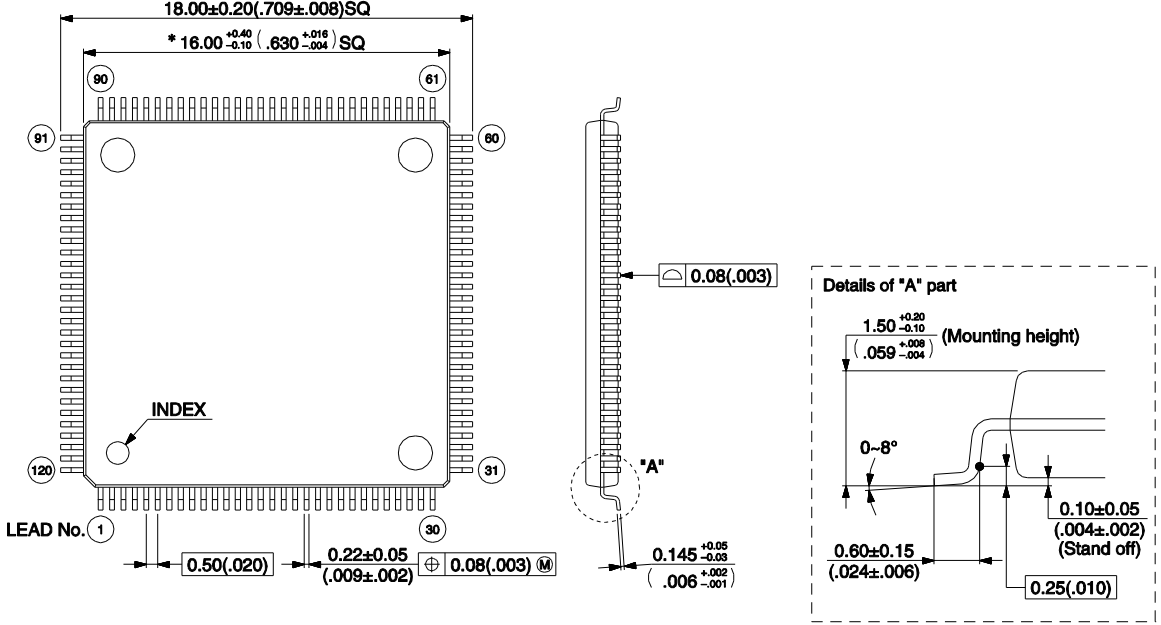
**12. Ordering Information**

Part Number	On-Chip Flash Memory	On-Chip SRAM	AES Calculator	Package	Packing
S6E1B84E0AGV20000	304	32	N/A	Plastic • LQFP (0.50 mm pitch), 80 pins (FPT-80P-M21)	Tray
S6E1B86E0AGV20000	560	64			
S6E1B84EHAGV20000	304	32	Yes		
S6E1B86EHAGV20000	560	64			
S6E1B84F0AGV20000	304	32	N/A	Plastic • LQFP (0.50 mm pitch), 100 pins (FPT-100P-M20)	Tray
S6E1B86F0AGV20000	560	64			
S6E1B84FHAGV20000	304	32	Yes		
S6E1B86FHAGV20000	560	64			
S6E1B84G0AGV20000	304	32	N/A	Plastic • LQFP (0.50 mm pitch), 120 pins (FPT-120P-M21)	Tray
S6E1B86G0AGV20000	560	64			
S6E1B84GHAGV20000	304	32	Yes		
S6E1B86GHAGV20000	560	64			

**13. Package Dimensions**

<p style="text-align: center;">120-pin plastic LQFP</p>  <p style="text-align: center;">(FPT-120P-M21)</p>	Lead pitch	0.50 mm
	Package width × package length	16.0 × 16.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.88 g
	Code (Reference)	P-LFQFP120-16×16-0.50

**120-pin plastic LQFP**  
(FPT-120P-M21)



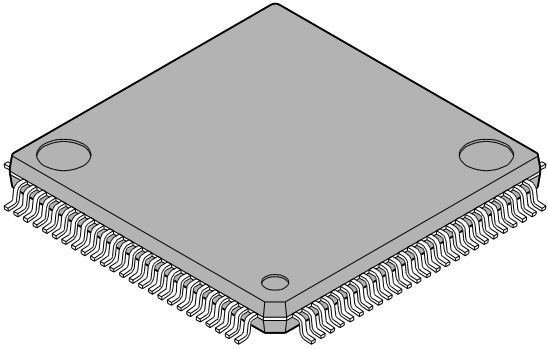
Note 1) \* : These dimensions do not include resin protrusion.  
Resin protrusion is +0.25(.010) MAX(each side).

Note 2) Pins width and pins thickness include plating thickness.

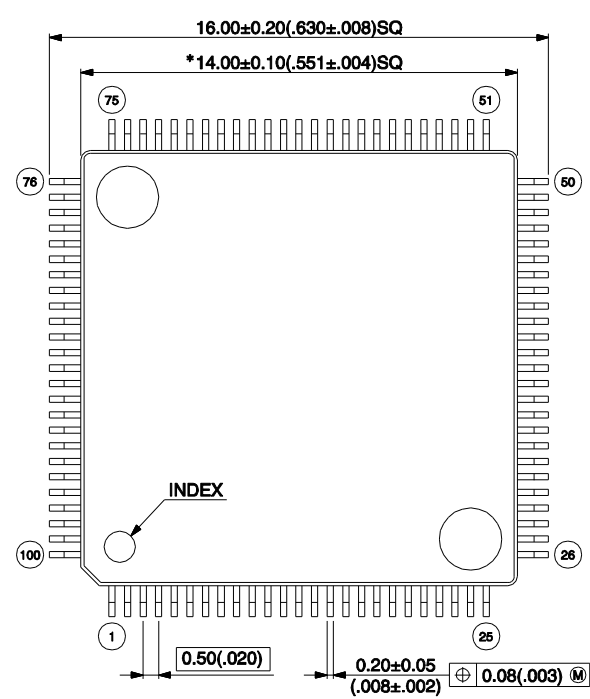
Note 3) Pins width do not include tie bar cutting remainder.

© 2002-2010 FUJITSU SEMICONDUCTOR LIMITED F120033S-c-4-7

Dimensions in mm (inches).  
Note: The values in parentheses are reference values.

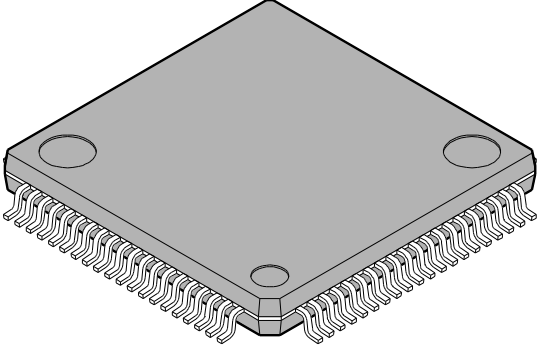
<p><b>100-pin plastic LQFP</b></p>  <p><b>(FPT-100P-M20)</b></p>	<b>Lead pitch</b>	0.50 mm
	<b>Package width × package length</b>	14.0 mm × 14.0 mm
	<b>Lead shape</b>	Gullwing
	<b>Sealing method</b>	Plastic mold
	<b>Mounting height</b>	1.70 mm Max
	<b>Weight</b>	0.65 g
	<b>Code (Reference)</b>	P-LFQFP100-14×14-0.50

**100-pin plastic LQFP (FPT-100P-M20)**

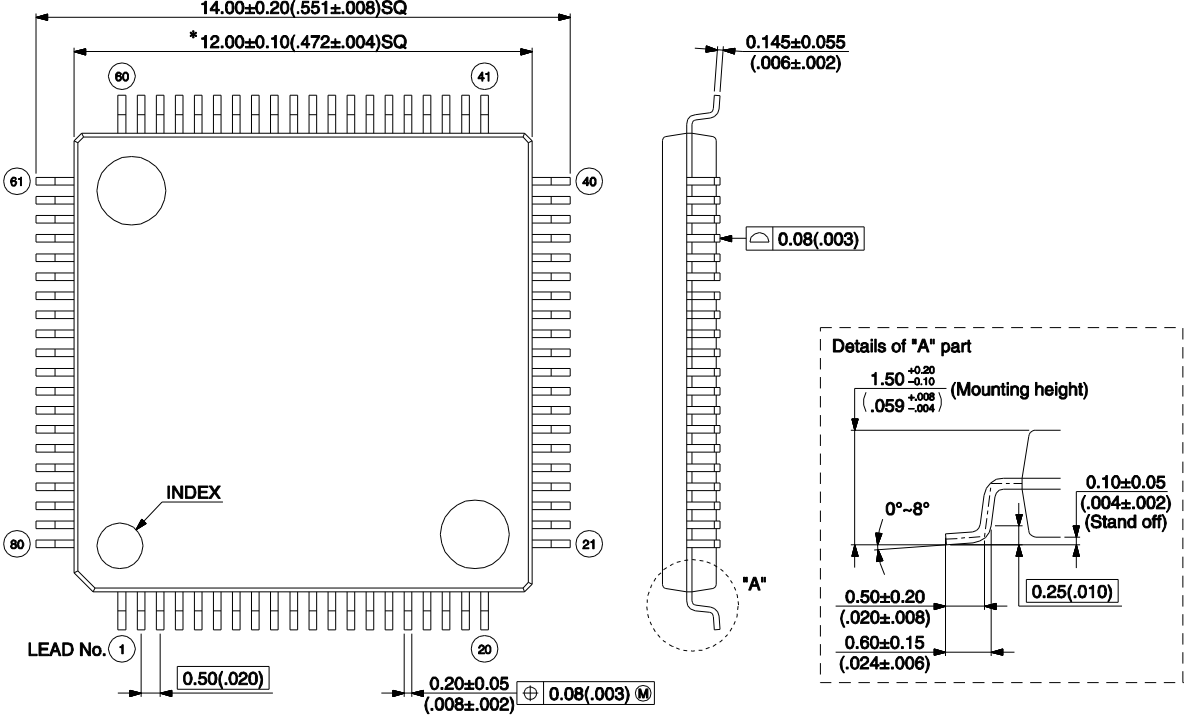


Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.

Dimensions in mm (inches).  
 Note: The values in parentheses are reference values

<p style="text-align: center;"><b>80-pin plastic LQFP</b></p>  <p style="text-align: center;"><b>(FPT-80P-M21)</b></p>	<b>Lead pitch</b>	<b>0.50 mm</b>
	<b>Package width × package length</b>	<b>12 mm × 12 mm</b>
	<b>Lead shape</b>	<b>Gullwing</b>
	<b>Sealing method</b>	<b>Plastic mold</b>
	<b>Mounting height</b>	<b>1.70 mm Max</b>
	<b>Weight</b>	<b>0.47 g</b>
	<b>Code (Reference)</b>	<b>P-LFQFP80-12×12-0.50</b>

**80-pin plastic LQFP (FPT-80P-M21)**



**Note 1) \* :** These dimensions do not include resin protrusion.  
**Note 2)** Pins width and pins thickness include plating thickness.  
**Note 3)** Pins width do not include tie bar cutting remainder.

Dimensions in mm (inches).  
 Note: The values in parentheses are reference values

© 2006-2010 FUJITSU SEMICONDUCTOR LIMITED F80035S-c-2-4

## Document History

Document Title: S6E1B8 Series 32-bit ARM® Cortex®-M0+ FM0+ Microcontroller

Document Number: 001-99223

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	4889752	TEKA	08/31/2015	New Spec.

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

#### Products

<a href="#">Automotive</a>	<a href="http://cypress.com/go/automotive">cypress.com/go/automotive</a>
<a href="#">Clocks &amp; Buffers</a>	<a href="http://cypress.com/go/clocks">cypress.com/go/clocks</a>
<a href="#">Interface</a>	<a href="http://cypress.com/go/interface">cypress.com/go/interface</a>
<a href="#">Lighting &amp; Power Control</a>	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a>
<a href="#">Memory</a>	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
<a href="#">PSoC</a>	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>
<a href="#">Spansion Products</a>	<a href="http://spansion.com/products">spansion.com/products</a>

#### PSoC® Solutions

[psoc.cypress.com/solutions](http://psoc.cypress.com/solutions)

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#)

#### Cypress Developer Community

[Community](#) | [Forums](#) | [Blogs](#) | [Video](#) | [Training](#)

#### Technical Support

[cypress.com/go/support](http://cypress.com/go/support)

Cypress, the Cypress logo, Spansion®, the Spansion logo, MirrorBit®, MirrorBit® Eclipse™, ORNAND™, Easy DesignSim™, Traveo™ and combinations thereof, are trademarks and registered trademarks of Cypress Semiconductor Corp. ARM and Cortex are the registered trademarks of ARM Limited in the EU and other countries. All other trademarks or registered trademarks referenced herein are the property of their respective owners.

© Cypress Semiconductor Corporation, 2015. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

This Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.